AD-A187 319 DESIGN AND IMPLEMENTATION OF A FIBER OPTIC RS232 LINK (U) NAVAL POSTGRADUATE SCHOOL MONTEREY CA J W RYAN SEP 87 1/1

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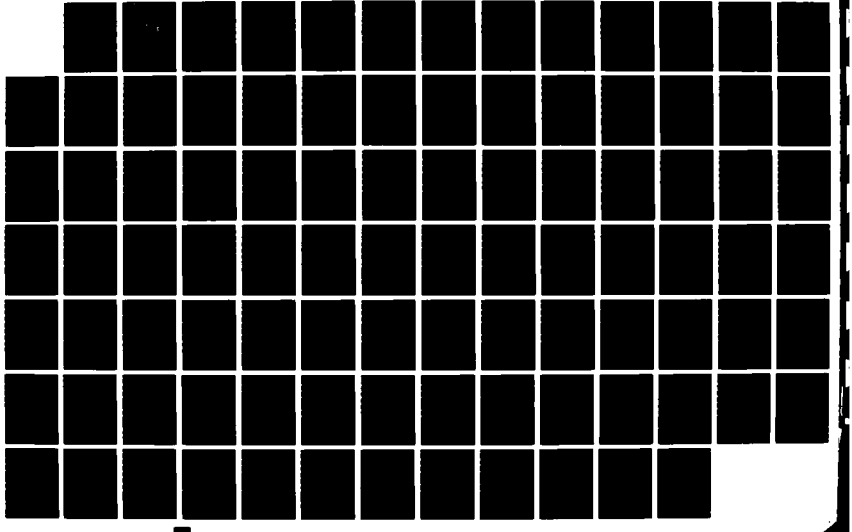

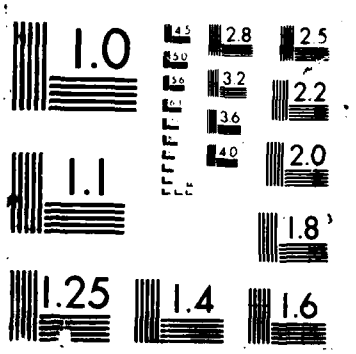
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NAVAL POSTGRADUATE SCHOOL

Monterey, California

THESIS

DESIGN AND IMPLEMENTATION OF A
FIBER OPTIC RS232 LINK

by

James William Ryan

September 1987

Thesis Advisor: John P. Powers

A187 319

SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a REPORT SECURITY CLASSIFICATION: UNCLASSIFIED	1b RESTRICTIVE MARKINGS
2a SECURITY CLASSIFICATION AUTHORITY	3 DISTRIBUTION/AVAILABILITY OF REPORT: Approved for public release; distribution is unlimited
2b DECLASSIFICATION/DOWNGRADING SCHEDULE	
4 PERFORMING ORGANIZATION REPORT NUMBER(S)	5 MONITORING ORGANIZATION REPORT NUMBER(S)
6a NAME OF PERFORMING ORGANIZATION: Naval Postgraduate School; 6b OFFICE SYMBOL (If applicable): 62	7a NAME OF MONITORING ORGANIZATION: Naval Postgraduate School
6c ADDRESS (City, State, and ZIP Code): Monterey, California 93943-5000	7b ADDRESS (City, State, and ZIP Code): Monterey, California 93943-5000
8a NAME OF FUNDING/SPONSORING ORGANIZATION; 8b OFFICE SYMBOL (If applicable)	9 PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c ADDRESS (City, State, and ZIP Code)	10 SOURCE OF FUNDING NUMBERS: PROGRAM ELEMENT NO; PROJECT NO; TASK NO; WORK UNIT ACCESSION NO

11 TITLE (Include Security Classification): Design and Implementation of a Fiber Optic RS232 Link

12 PERSONAL AUTHOR(S): Ryan, James W.

13a TYPE OF REPORT: Master's Thesis	13b TIME COVERED: FROM ____ TO ____	14 DATE OF REPORT (Year Month Day): 1987 September	15 PAGE COUNT: 93

16 SUPPLEMENTARY NOTATION

17 COSATI CODES			18 SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	Fiber Optics, RS232, Optical Link

19 ABSTRACT (Continue on reverse if necessary and identify by block number)

This thesis investigates the feasibility of using a bi-directional fiber optic link to implement a RS232 data link. The results showed that a fiber optic link is a viable replacement. It offers a bandwidth up to 5 MHz, 250 times that of a RS232 data link. This fiber optic link was implemented over a distance of 1.5 kilometers, nearly 100 times that of the present RS232 link. It also offers the benefits of space and weight savings and is comparable to devices produced commercially but at a substantial cost savings.

20 DISTRIBUTION/AVAILABILITY OF ABSTRACT: ☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS	21 ABSTRACT SECURITY CLASSIFICATION: UNCLASSIFIED
22a NAME OF RESPONSIBLE INDIVIDUAL: John P. Powers	22b TELEPHONE (Include Area Code): 408-646-2200; 22c OFFICE SYMBOL: 62

DD FORM 1473, 84 MAR — 83 APR edition may be used until exhausted; All other editions are obsolete — SECURITY CLASSIFICATION OF THIS PAGE

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Design and Implementation of a Fiber Optic RS232 Link

by

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Lieutenant, United States Navy
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Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
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ABSTRACT

This thesis investigates the feasibility of using a bi-directional fiber optic link to implement a RS232 data link. The results showed that a fiber optic link is a viable replacement. It offers a bandwidth up to 5 MHz, 250 times that of a RS232 data link. This fiber optic link was implemented over a distance of 1.5 kilometers, nearly 100 times that of the present RS232 link. It also offers the benefits of space and weight savings and is comparable to devices produced commercially but at a substantial cost savings.

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I. INTRODUCTION

This thesis investigates replacing the RS232 electronic link with a fiber optic link. The primary objectives were an investigation of the practical problems associated with connecting two noncompatible devices together and then to implement these connections onto a fiber optic link.

A. PURPOSE

The implementation of a fiber optic link offers several distinct advantages over an electrical one. First the fiber and the supporting circuitry would require less space and would weigh less than an electronic link. The increased bandwidth offered by a fiber optic link would offer the user the possibility of system expansion. Utilizing fibers would virtually eliminate the problem of crosstalk which can occur when two wires are close enough to each other to allow signals from one line to cross over to another as a result of electromagnetic interference (EMI). [Ref. 1]

The fiber optic link proposed here is full duplex bidirectional over a single fiber. The link achieves this capability by utilizing a wavelength division multiplexing scheme. In wavelength division multiplexing several optical signals of differing wavelengths are coupled into a single fiber [Ref. 2].

Wavelength division multiplexing is achieved in this project through the use of a dichroic filter. As seen in Figure 1.1 a dichroic filter allows the transmission of one wavelength while reflecting the other wavelength. Specifically, a light wave, generated by an LED, transmits through the filter and is directed into the fiber optic cable. A light wave, which is generated in the same fashion at the other end of the fiber, reflects off of the dichroic filter and into a PIN detector. A complete analysis of light generation and reception is found in Chapter III.

B. RESULTS

The researched showed that the link investigated in this thesis is realizable and it was found to be comparable to units on the commercial market. A detailed analysis of the system performance is found in Chapter IV.

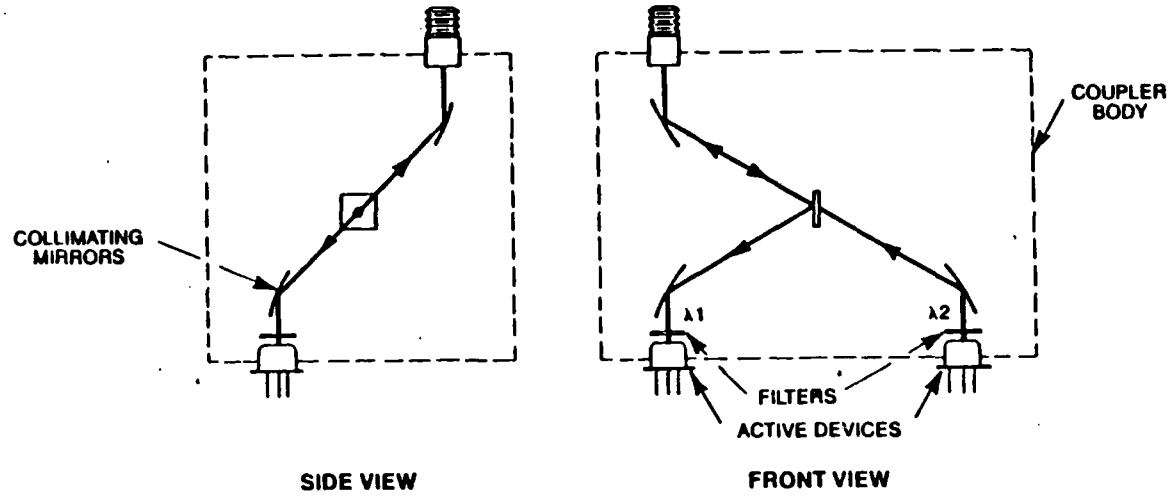


Figure 1.1 Light Transmission Scheme. [Ref. 3]

II. BACKGROUND

A. THE RS232 INTERFACE

In order for two devices to communicate, they must be connected in such a way so that electrical signals are transmitted and received correctly by each unit.

This connection may be achieved directly by connecting wires to the devices or by using an intermediate medium. More often than not, the telephone network is used as this medium. The most widely used connection to link the medium to the device is the RS232 data link. [Ref. 4:p.167]

The RS232 link was originally designed to allow communications between data terminal equipment (DTE) (i.e., computers) and data communication equipment (DCE) (e.g., modems) [Ref. 5:p. 11]. For the application discussed in this project two DTEs will be connected without the use of DCEs. This configuration is called null modem [Ref. 5:p. 13].

When this is done, a problem often arises. The DTEs cannot communicate with each other as the pin configurations of the RS232 were designed to be connected to DCEs. It would seem as if all one would have to do is cross-connect the pins. However this is not the case, as the manufacturers designate the pins of the RS232 to suit their own needs. To find these

cross-connections required is sometimes a very frustrating and time consuming venture.

In an effort to make equipment from different manufacturers compatible the Electronic Industries Association, (EIA), published a standard, the RS232-C. Unfortunately this standard specifies the connections between DTEs and DCEs. Specifically it delineates the electrical characteristics of the circuits between the two devices and the names and numbers of the pins necessary for connection to allow communications.

The pins numbers and titles as specified by the EIA are listed in Table I. Since this project is concerned only with null modem configurations, not all the pins listed will be discussed in this project.

While the RS232 link is an extremely useful interface it has an potential ground loop problem. Because of this and other prob-lems, the standard recommends that the cable interconnection between the two devices should be limited to a maximum dis-tance of 50 feet; at longer distances the connection becomes unreliable and hazardous. [Ref. 4:p. 168]

Another major problem with the use of the RS232 is that large signal voltages are required to insure noise immunity is achieved on the link. The RS232 signal voltages are anywhere between plus and minus 25 volts. These high transmission voltages are required because of common mode noise. This noise could be on the level of a few volts. Some of the sources of the common mode noise could be from photocopiers, typewriters,

TABLE I

EIA RS232 STANDARDS

Pin number	Circuit	Description
1	AA	Protective ground
2	BA	Transmitted data
3	BB	Received data
4	CA	Request to send
5	CB	Clear to send
6	CC	Data set ready
7	AB	Signal ground (common return)
8	CF	Received line signal detector
9	—	(Reserved for data set testing)
10	—	(Reserved for data set testing)
11		Unassigned
12	SCF	Secondary received line signal detector
13	SCB	Secondary clear to send
14	SBA	Secondary transmitted data
15	DB	Transmission signal element timing (DCE source)
16	SBB	Secondary received data
17	DD	Receiver signal element timing (DCE source)
18		Unassigned
19	SCA	Secondary request to send
20	CD	Data terminal ready
21	CG	Signal quality detector
22	CE	Ring indicator
23	CH/CI	Data signal rate selector (DTE/DCE source)
24	DA	Transmit signal element timing (DTE source)
25		Unassigned

[Ref. 6:p. 80]

printers, etc. Even if a link of greater than 50 feet could be safely achieved, one would find that a build up of capacitance is present, which would severely affect the quality of the signal as it transitions between the positive and negative voltages. [Ref. 5:p. 14]

Another limiting feature of the RS232 interface is that, even with these high voltage levels that the EIA standard specifies the interface is rated for a signaling rate from d.c. to an upper limits of only 20K bits per second.[Ref. 6:p. 79]

B. PROPOSED FIBER OPTIC LINK

The proposed fiber optic link presented in this project would eliminate problems inherent in the RS232 link. This link would increase the distances between DTEs almost 100 fold and increase bandwidth to that of 250 times to that of the RS232.

The applications for a link such as this one are numerous. It opens the possibility of data transfer simplification, weight reduction of the link, communications link security, and the expansion to a LAN (local area network).

The link described here is full duplex over a single fiber. In a full duplex mode both DTEs can be transmitting simultaneously. In other fiber optic links simultaneous transmission was only possible by using two fibers, one for transmission and one for reception. To achieve a single fiber scheme the two light signals must be multiplexed onto one

fiber. The multiplexing method used for this link is wavelength division multiplexing (WDM).

WDM is obtained through the use of a coupler manufactured by ADC FIBER OPTICS. This coupler is called a Connectorized Active Full Duplex Coupler (CAF) [Ref. 7:p. 1]. A diagram of the operation of this coupler is shown in Figure 2.1. As can seen there are two LEDs transmitting at two differing wavelengths. The light signal transmitting at 865 nanometers will be detailed as an example as the transmission and reception of the other wavelength of 730 nanometers is similar. The electronic signal generated by the DTE is converted to a light signal by the 865 nanometer LED, (a detailed analysis of this process is found in chapter 3), the light wave passes through a dichroic filter, which passes that wavelength, and is reflected into the fiber by a focusing mirror. As the light exits the fiber at the other end it is incident upon another focusing mirror which directs the light wave onto another dichroic filter. This dichroic filter is set to transmit the light 730 nanometer causing the light at 865 nanometers to be reflected into the PIN detector. From the detector the light wave is converted to an electrical signal.

The CAF described above is an integral element of the fiber optic modules used in this link; a diagram of these modules is shown in Figure 2.2. The three major components of are: the transmitting circuitry, the receiver circuitry and the CAF. The basic operation for the modules is that the

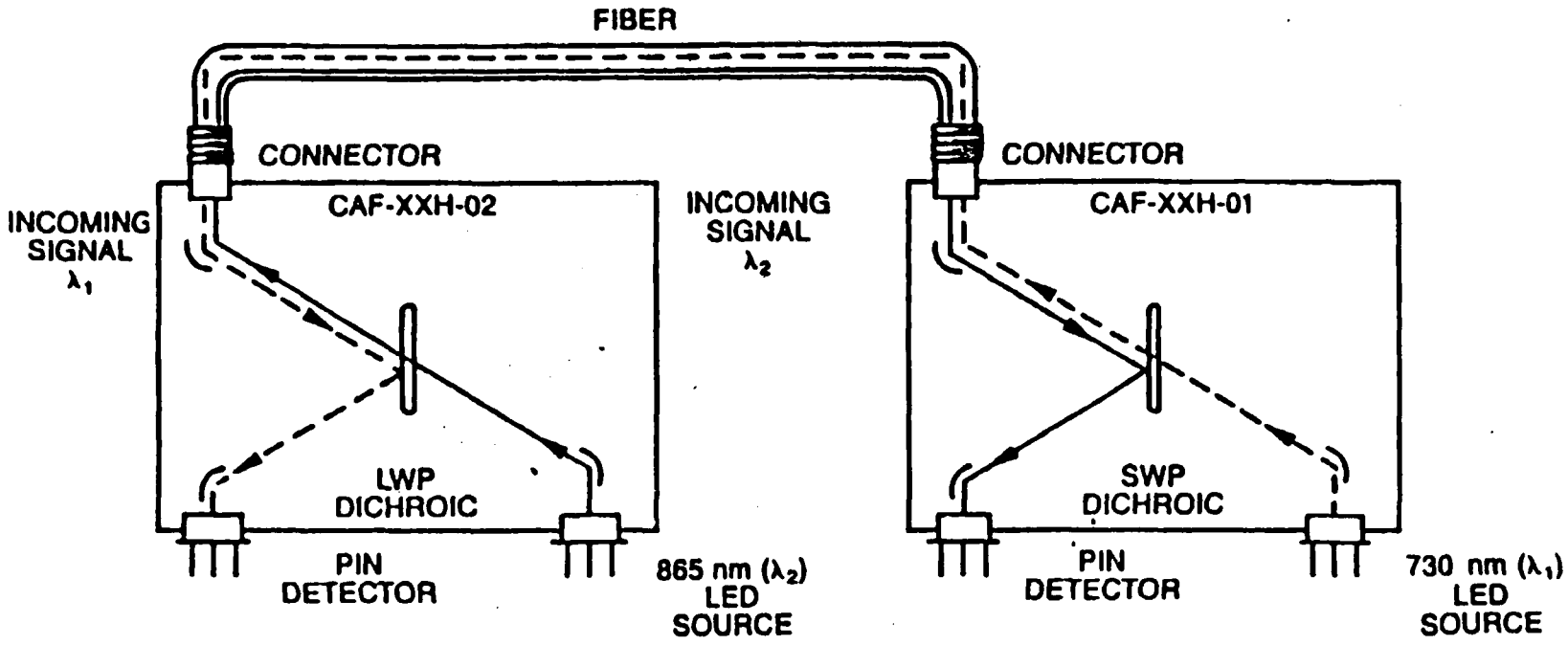


Figure 2.1 CAF [Ref. 7:p. 5]

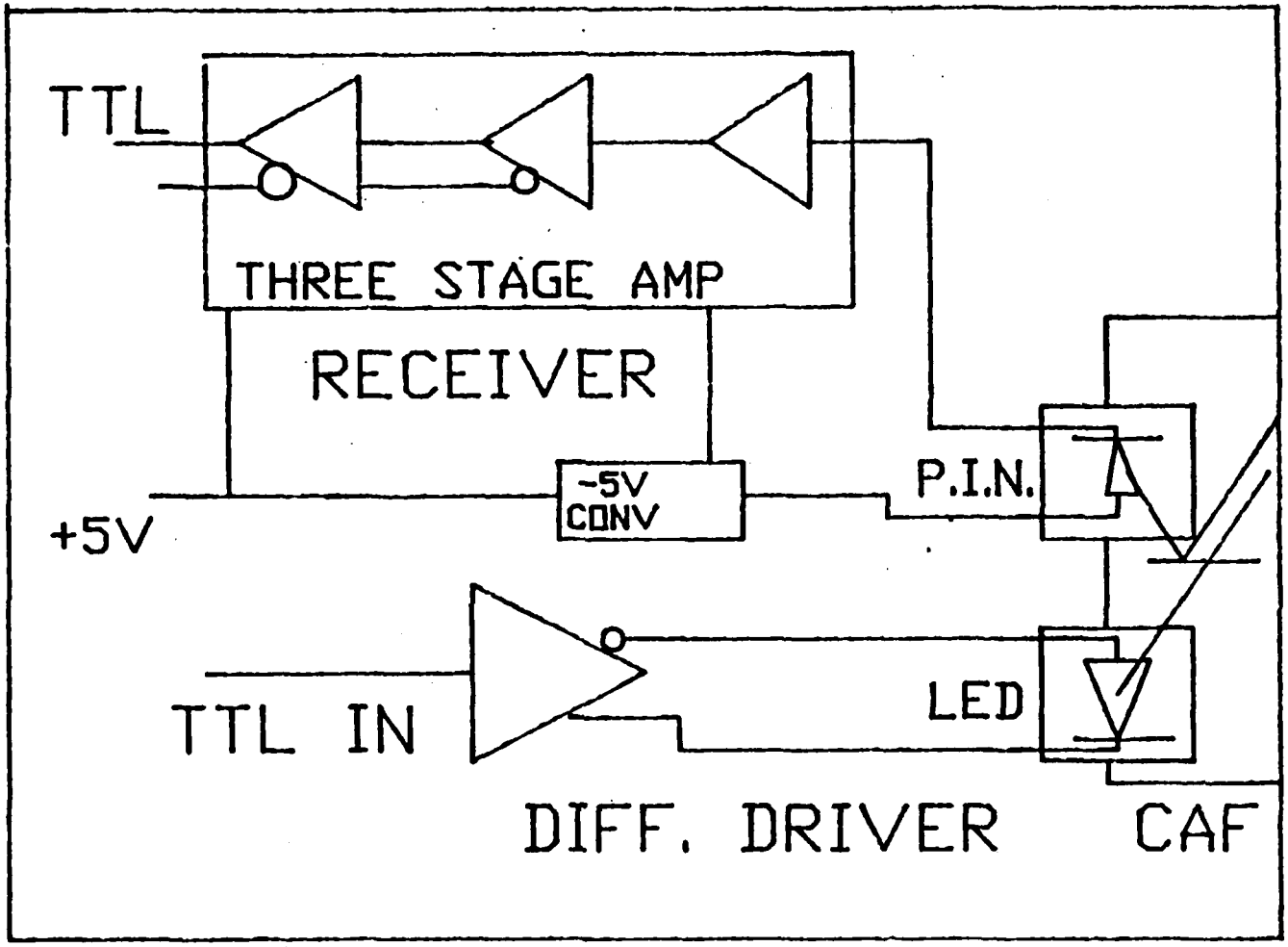


Figure 2.2 Fiber Optic Module [Ref. 7:p. 3]

incoming electrical signal drives current through the LED in the CAF, sending a light wave into fiber which is received by the PIN detector in the other CAF. The light wave is converted to an electrical signal and through the use of a three stage amplifier is set to an acceptable level. Detailed analysis of transmitting and receiving circuitry is given in Chapter III.

III. IMPLEMENTED FIBER OPTIC LINK

A. CROSS CONNECTIONS OF THE RS232

The first step in this project was to connect a Hewlett-Packard Series 85 personal computer (HP-85) to a NEC SPINWRITER model 7710 printer (NEC). Following successful operation the next step was to connect the HP-85 to an AMPEX 210 Video display terminal (AMPEX), in a null modem configuration. The functions of the HP-85, NEC, and the AMPEX RS232 pins are listed in Tables II, III, and IV, respectively. The reader is referred to section A of Chapter II for formal definitions of these pins. The problem of connecting the DCEs in a null modem configuration proved to be a most formidable one, since manufacturers fail to adhere to any real consistencies in their standards of their RS232 pin functions.

The cross connections necessary for transmission of the data and for the handshaking between the two DTE's are shown in Figures 3.1 and 3.2. Figure 3.1 shows the minimum connections necessary for proper communication between the HP-85 and the NEC. The direction of signal flow and the manufacturers pin titles are also listed in the figure. Figure 3.2 shows the minimum connections of the RS232 required for proper operation between the HP-85 and AMPEX. The pin titles and direction of data flow are also shown.

TABLE II

HP-85 RS232 PINS

PIN	FUNCTION
1.	EQUIPMENT GROUND
2.	TRANSMITTED DATA
3.	RECEIVED DATA
4.	REQUEST TO SEND (RTS)
5.	CLEAR TO SEND (CTS)
6.	DATA SET READY (DSR)
7.	SIGNAL GROUND
8.	RECEIVED LINE SIGNAL DETECTOR
12.	SECONDARY RECEIVED LINE SIGNAL DETECTOR
13.	SECONDARY CLEAR TO SEND
14.	SECONDARY TRANSMITTED DATA
15.	TRANSMITTER SIGNAL ELEMENT TIMING
16.	SECONDARY RECEIVER DATA
17.	RECEIVER SIGNAL ELEMENT TIMING
19.	SECONDARY REQUEST TO SEND
20.	DATA TERMINAL READY (DTR)
21.	SIGNAL QUALITY DETECTOR
22.	RING INDICATOR
23.	DATA SIGNAL RATE SELECTOR
24.	TRANSMIT SIGNAL ELEMENT TIMING

[Ref. 8:p. 47]

TABLE III

NEC RS232 PINS

PIN	FUNCTION
1.	EQUIPMENT GROUND
2.	TRANSMITTED DATA
3.	RECEIVED DATA
4.	REQUEST TO SEND (RTS)
5.	CLEAR TO SEND (CTS)
6.	DATA SET READY (DSR)
7.	SIGNAL GROUND
8.	CARRIER DETECT
19.	REVERSE CHANNEL
20.	DATA TERMINAL READY (DTR)
23.	PAPER OUT / RIBBON END

[Ref. 9:p. 3-5]

TABLE IV

AMPEX RS232 PINS

PIN	FUNCTION
1.	EQUIPMENT GROUND
2.	TRANSMITTED DATA
3.	RECEIVE DATA
4.	REQUEST TO SEND (RTS)
5.	CLEAR TO SEND (CTS)
6.	DATA SET READY (DSR)
7.	SIGNAL GROUND
8.	DATA CARRIER DETECT (DCD)
20.	DATA TERMINAL READY (DTR)

[Ref. 10:p. 21]

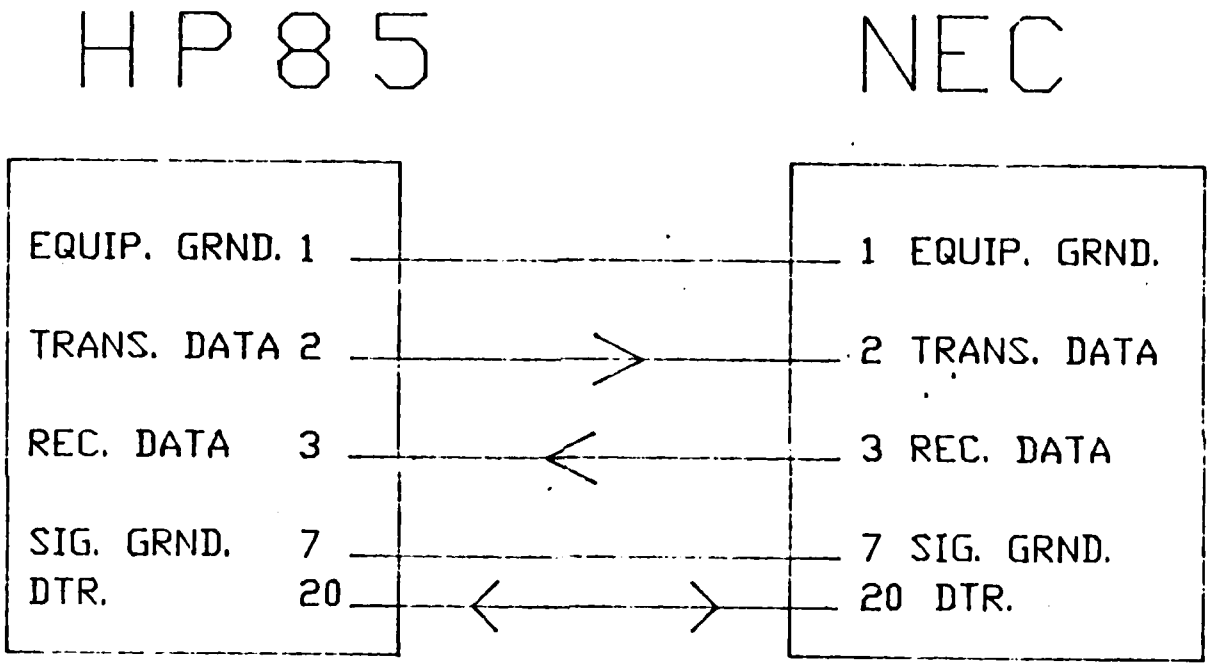


Figure 3.1 HP-85 / NEC Connection

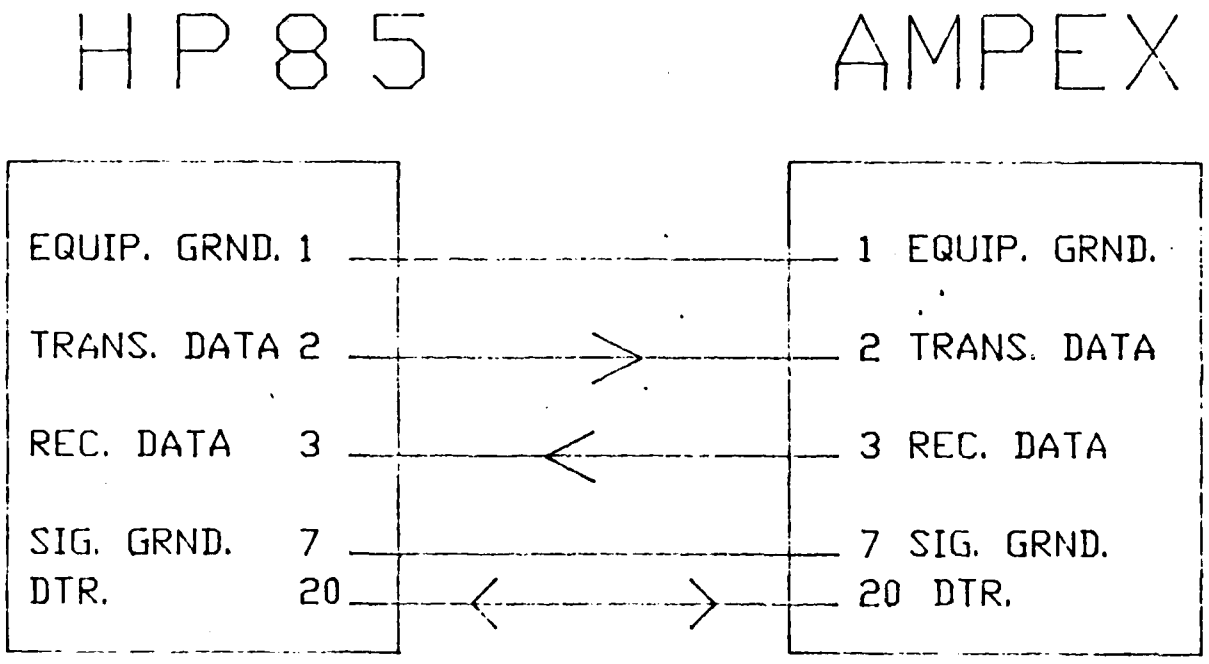


Figure 3.2 HP-85 / AMPEX Connection

The second step of this project was to determine which were the data transmission pins and the data reception pins and the pins required for the handshaking. Two pins are readily identifiable. Pin 1 is the chassis ground and pin 7 the signal ground. This is true for both configurations.

Considering the connection between the HP-85 and the NEC, pin 3 of the HP-85 is used to transmit the data to the receive pin of the NEC which is also pin 3. The NEC uses pin 2 to transmit a break signal back to the HP-85. This signal, of 300 - 700 milliseconds duration, is interpreted by the HP-85 as a priority interrupt [Ref. 9:p. 4-5]. Once this signal is received, the HP-85 ceases transmission of the data. The break signal is transmitted when any of the following conditions occur [Ref. 9:p. 4-6]:

1. paper out
2. buffer overflow
3. ribbon end

When the above situations have been rectified, the NEC transmits another signal of the same duration as the break signal and transmission of the data will occur [Ref. 9:p. 4-6]. Pin 20 is Data Terminal Ready (DTR) line; this is a handshaking line, where a positive voltage indicates that the DTEs are ready to begin transmission [Ref. 6:p. 84].

For the configuration of the HP-85 connected to the AMPEX terminal, pin 3 was determined to be the receive channel of the AMPEX and pin 2 the transmit data from the AMPEX. Pin 20 is the DTR line here also.

Now that the data lines and handshaking pins have been identified, the next step was to circumvent the handshaking lines. The DTR lines of both configurations are connected to a high voltage and the ground lines are connected to an absolute ground. After doing this we will have two data channels: one transmit and one receive. We now have the desired configuration for transmission on the fiber optic link.

B. TRANSMISSION OF THE LIGHT SIGNAL

To transmit the signal on the link the bipolar voltage levels used by the RS232 are converted to TTL levels. On data lines 2 and 3, a positive level voltage (SPACE) corresponds to a logical zero and a negative voltage level (MARK) corresponds to logical one [Ref. 5:p. 14]. The voltage levels used by the HP-85 to indicate a logical "1" and a logical "0" are shown in Figure 3.3. Figure 3.3 shows that the HP-85 interprets voltages between positive 5 volts and positive 15 volts as a logical "0" and the voltages between negative 5 and negative 15 volts as a logical "1". The voltage levels used by the NEC are shown in Figure 3.4. Figure 3.4 shows that the NEC interprets voltages between 0 and positive 12 volts as a logical "0" and the voltages between 0 and negative 12 volts as a logical "1". The voltage levels used by the AMPEX could not be referenced. It was assumed that voltages between +5 volts and +15 volts will be interpreted as a SPACE and voltages between -5 volts and -15 volts as a MARK. Since the

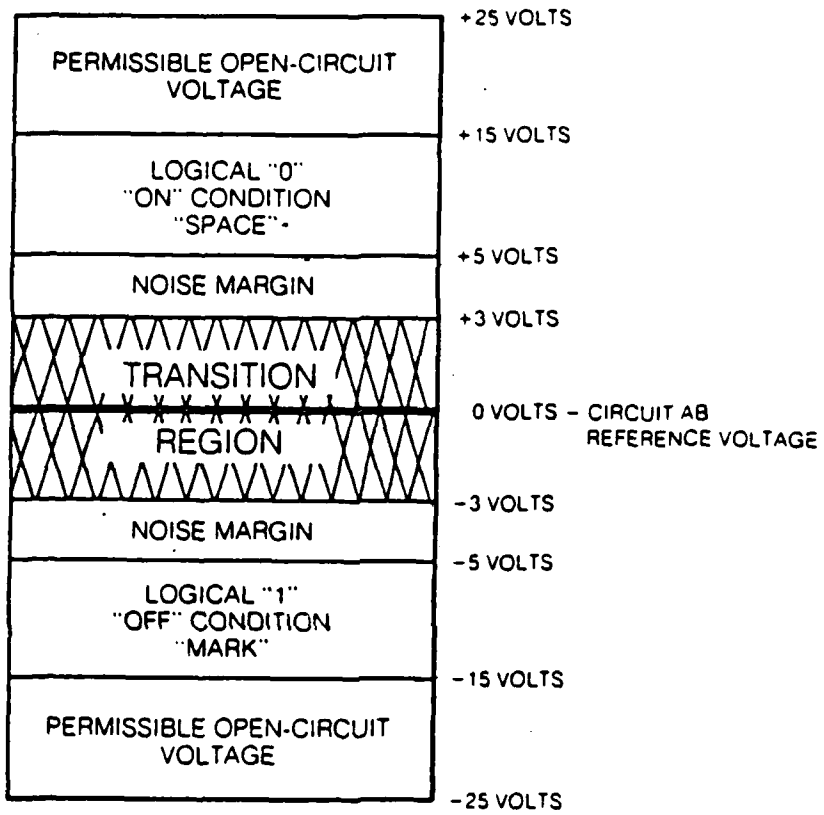


Figure 3.3 HP-85 RS232 Voltage Levels [Ref. 8:p. 45]

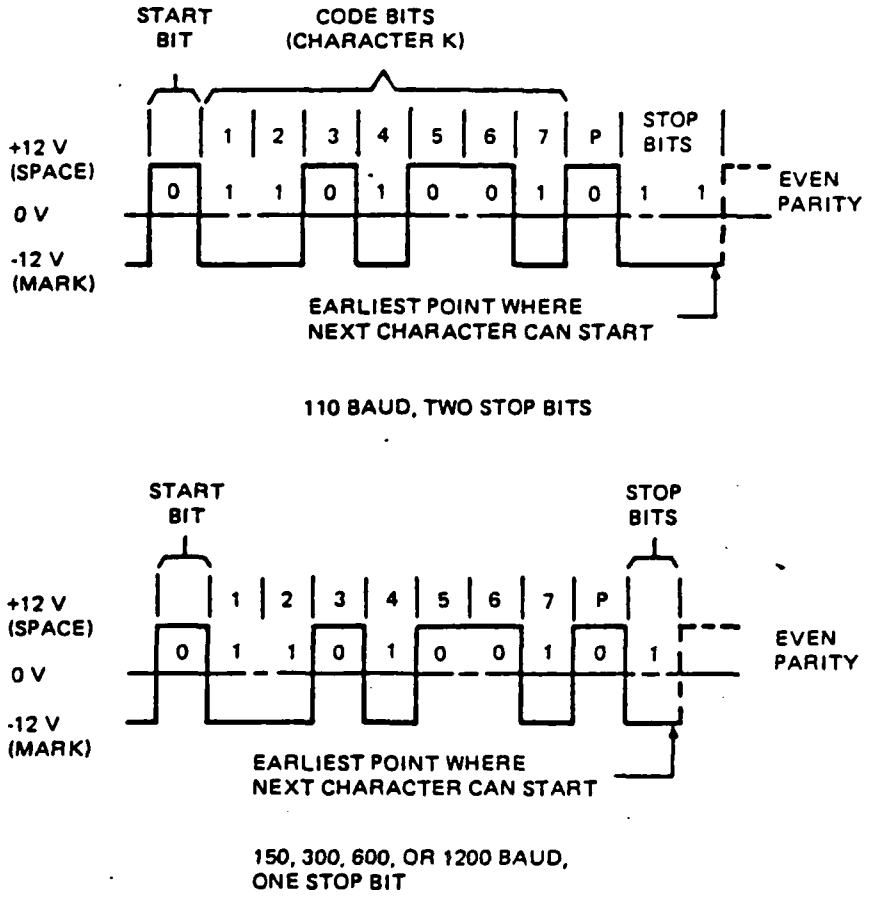


Figure 3.4 NEC RS232 Voltage Levels [Ref. 9:p. 4-1]

voltage levels are bipolar they have to be converted to TTL levels required for the fiber optic modules. The device utilized for the conversion is the MC1489, a quad line receiver [Ref. 11:p. 5-120] (Appendix A). The MC1489 interprets voltages between -3 and -25 volts as a logical "1" and voltages between +3 and +25 volts as a logical "0" [Ref. 5:p. 5-121]. The output voltage range from the MC1489 is 2.5 to 5.0 volts for logical "1" and 0 to 0.45 for logical "0" [Ref. 11:p. 5-121]. The TTL outputs from the MC1489 are supplied to the transmitter circuitry of the fiber optic module.

The function of the transmitter circuitry is to modulate the LED of the CAF on or off in accordance with the input signal. The circuitry is shown in Figure 3.5. As Figure 3.5 shows, the TTL input is fed into two exclusive-or gates. On the first gate, U2A, one input is the TTL signal and the other input is always asserted high through a 1K ohm pull up resistor. On the second gate, U2B, one input is the TTL input signal and the other input is non-asserted through ground. By having this configuration, Q6 and Q7 are alternately driven on and off. When Q6 is asserted, it allows the LED to transmit a light signal through the fiber. When Q7 is asserted, current is drawn through resistor R15. This design has the advantage that the power supply output remains constant and transient emissions are minimized. Diodes D1, D2, and D3,are used to set the bias on the base of Q8. Diodes, instead of resistors, are

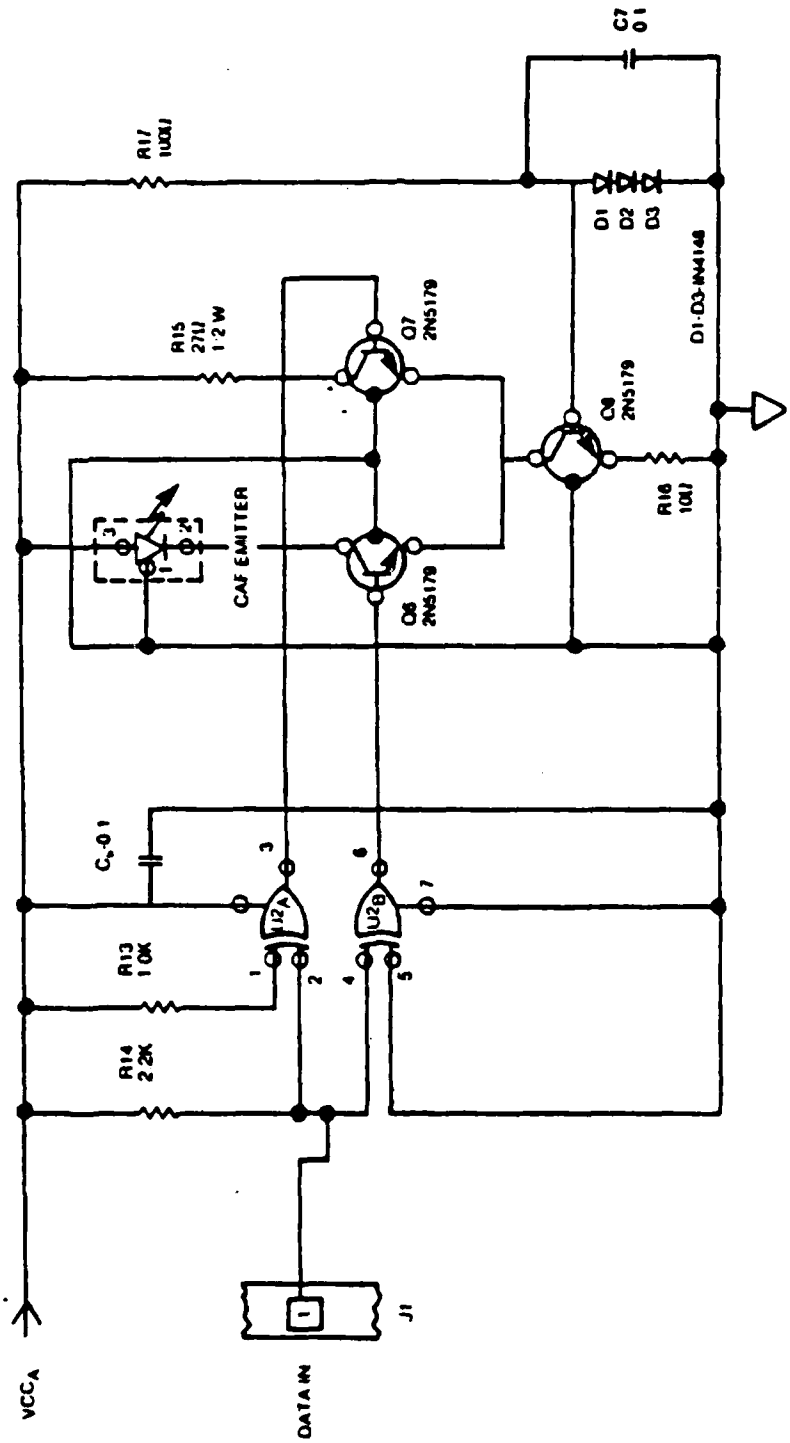


Figure 3.5 Transmitter [Ref. 7:p. 7]

used so that a constant drive current will be maintained during power fluctuations. [Ref. 7:p. 6]

C. RECEPTION OF THE LIGHT SIGNAL

The light signal transmitted into the fiber is received by the pin detector in the CAF. The receiver circuitry is shown in Figure 3.6. The light signal received must be significantly amplified before it can be converted into a TTL signal. This is achieved in the receiver by three separate stages: a high gain feedback preamplifier, a low gain differential amplifier and a voltage comparator. [Ref. 7:p. 8]

The preamplifier is a three stage transistor amplifier. The transistor array used is CA3127E, a high frequency n-p-n transistor array (Appendix B). This stage converts the low current levels received by the pin detector into a voltage.

The signal out of the preamplifier is applied to a low gain differential amplifier. The purpose of this amplifier is to convert the input to a complementary differential output. The outputs of this stage are applied to a precision voltage comparator, a LT1016. This comparator performs the function of converting the differential analog input to TTL levels [Ref. 7:p. 8].

The TTL levels are then converted to bipolar level by a MC1488, a quad line driver (Appendix C). The MC1488 is designed to provide a complete interface between the DTEs and the DCEs [Ref. 11:p. 5-118]. The outputs are now suitable for use by the RS232. Once the bipolar levels are achieved, the

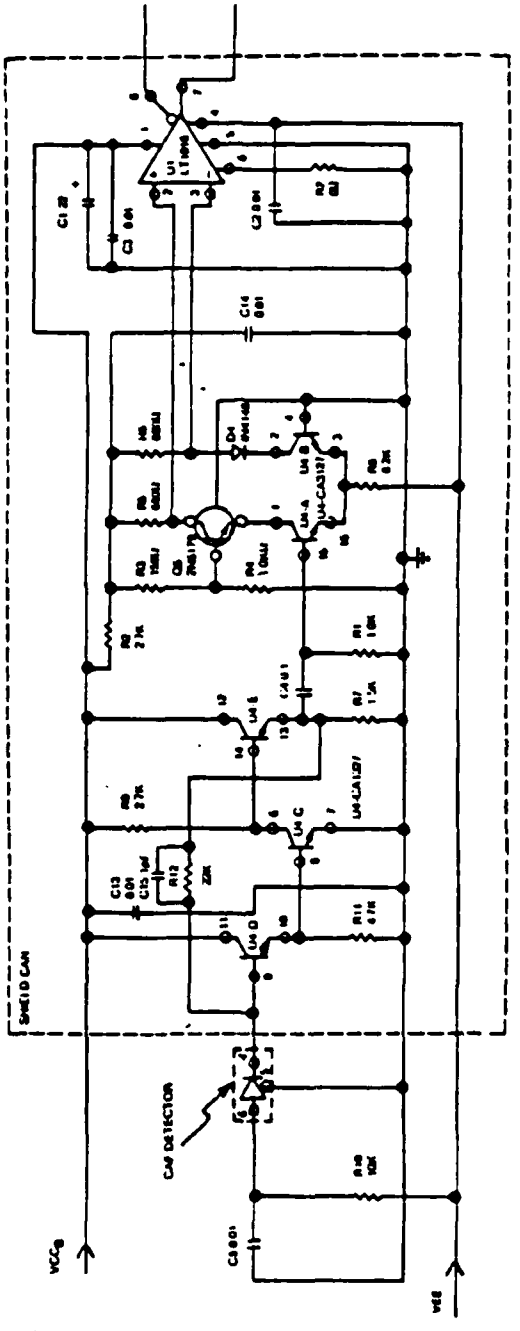


Figure 3.6 Receiver [Ref. 7:p. 7]

signals are routed back to the RS232 to complete the transmission path. The diagram of the system is shown in Figure 3.7. This figure shows the complete fiber optic link. The actual size of one of these units, including the connection for the RS232 port is 6 by 11 inches.

D. RECEIVER MODIFICATIONS

As has been seen, the main body of this project has been fiber optic modules. These modules were developed by ADC Fiber Optic Corporation. For our specific application modifications were required to suit our frequency range. The frequency range that the modules were designed for was from 0.4 MHz to 20 MHz for a total bandwidth of 19.6 MHz. Our required bandwidth is only 19.2 KHz, however the frequency range is from d.c. to 20 KHz. This is the bandwidth used by the RS232. It was therefore necessary to reduce the lower end of the frequency response of the modules.

Analysis of the transmitter and receiver circuits of the fiber optic modules revealed that in the receiver circuitry, there was a high pass filter between the high feedback preamplifier and the low gain differential amplifier. Referring to the receiver circuit schematic (Figure 3.6), capacitor C4 and resistor R1 act as a high pass filter with a cutoff frequency of 1592 Hz.

After reviewing the frequencies required for the configurations (HP-85 to NEC, HP-85 to AMPEX), it was found

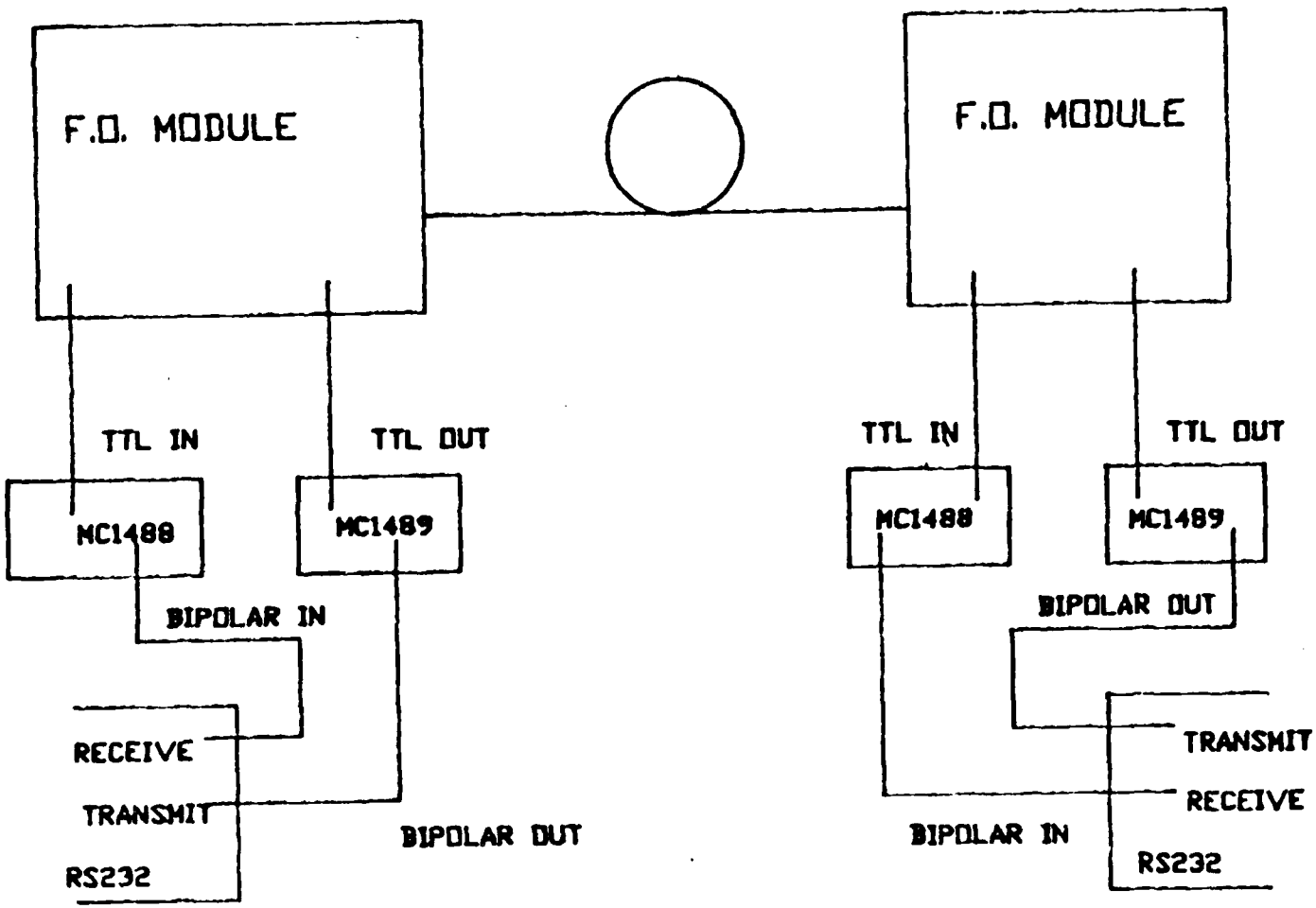


Figure 3.7 System Diagram

that the lowest frequency transmitted would be by the NEC, 1.43 Hz to 3.3 Hz for the break signal. The method to decrease the cutoff frequency was to place another capacitor in parallel with C4. This was determined to be the best solution as the space the circuit board of the modules is limited and the increased capacitance decreased the noise caused from high speed components.

The increased capacitance was calculated to be 111.4 microfarads. A 100 microfarad capacitor was placed in parallel with C4 to give a theoretical cutoff frequency of 1.59 Hz. After this addition was made to the receiver circuit (of both units), a full duplex bi-directional fiber optic link capable of handling the data flow of RS232 was achieved. Both the connections to the printer and to the terminal performed flawlessly.

IV. SYSTEM EVALUATION

Evaluation of the transmitted optical power, operating wavelengths, receiver sensitivity, cross talk levels, and lengths of possible links with fibers of different sizes and differing losses are examined in this chapter. In the section dealing with the transmitting optical both units will be examined, however in the other sections only one unit will be discussed as the data compiled for each unit was comparable to the other.

A. TRANSMITTED OPTICAL POWER

The measurement of the transmitted optical power was done by a Photodyne Model 22XL Optical Multimeter. Each fiber optic module was connected to the optical multimeter via three meters of 62.5/125 micrometer graded index fiber, provided by the manufacturer of the modules. In order to measure the power output a square wave was applied to each of the fiber optic modules. The square wave was generated by a Wavetek signal generator and verified by using an oscilloscope. The signal input frequency range was from 100 Hz to 1 MHz, i.e., the complete operating range of the optical multimeter [Ref. 12].

The unit containing the CAF transmitting at 730 nanometers transmitted a signal at -11.8 dbm (66.1 microwatts), while the CAF transmitting at 865 nanometers transmitted a signal of

-12.2 dbm (60.3 microwatts) to give a total power through the fiber, during duplex operation, of -8.98 dbm (126.4 microwatts). These measurements were made by connecting the optical multimeter directly to the CAF. The rated power through the fiber, at maximum capacity, is specified to be -10.0 dbm (100 microwatts) [Ref. 13]. It is assumed that the manufacturer rated his product conservatively to be safe.

B. OPERATING WAVELENGTHS

The system, as has been stated, has two LEDs transmitting at different wavelengths. The wavelength to be received is reflected off the dichroic filter and into the PIN detector, while the transmitted wavelength passes through the filter into the fiber. The operating wavelengths were measured to see if there was a possibility of crosstalk between the two wavelengths caused by an overlap of wavelengths from the LEDs.

The measurement of the wavelengths was accomplished by connecting the CAF to a Photodyne Model 1100XM Fiber Optic Spectral Analyzer and then to the optical multimeter.

For the CAF specified to transmit at 730 nanometers, the peak output wavelength was found to be 729 nanometers. The three db points were 717 nanometers and 745.5 nanometers, to give a half power bandwidth of 28 nanometers. The full operating range of this CAF was found to be from 688 nanometers to 771 nanometers, for total bandwidth of 83 nanometers.

The CAF specified to transmit at 865 nanometers had a peak output wavelength of 862.5 nanometers. The three db points were found to be at 843 nanometers and 874.5 nanometers, to give a half power bandwidth of 31.5 nanometers. The operating range of this CAF was found to be from 821 nanometers to 905 nanometers, for a bandwidth of 84 nanometers. Thus, there is a 50 nanometers separation between the two wavelengths.

C. RECEIVER SENSITIVITY LEVELS

The receiver sensitivity level of the PIN detector was specified, in the worst case, as -24.5 dbm. However it was observed that the detector was able to receive a signal at a level of -44.0 dbm and the receiver circuitry was able to convert it the original TTL signal. This represents an increase of 79.5% in the sensitivity level of the detector. It was also observed that, although a signal below -44.0 dbm could be received by the PIN detector, it would not have sufficient power to trigger a response from the first stage amplifier of the receiver circuitry.

D. CROSSTALK

Four crosstalk measurements were made on the fiber optic modules. These measurements were made with different components on and off the modules to see their effect on crosstalk.

A 1 MHz square wave was applied to the fiber optic modules. The 1 MHz frequency was chosen so that the effect of

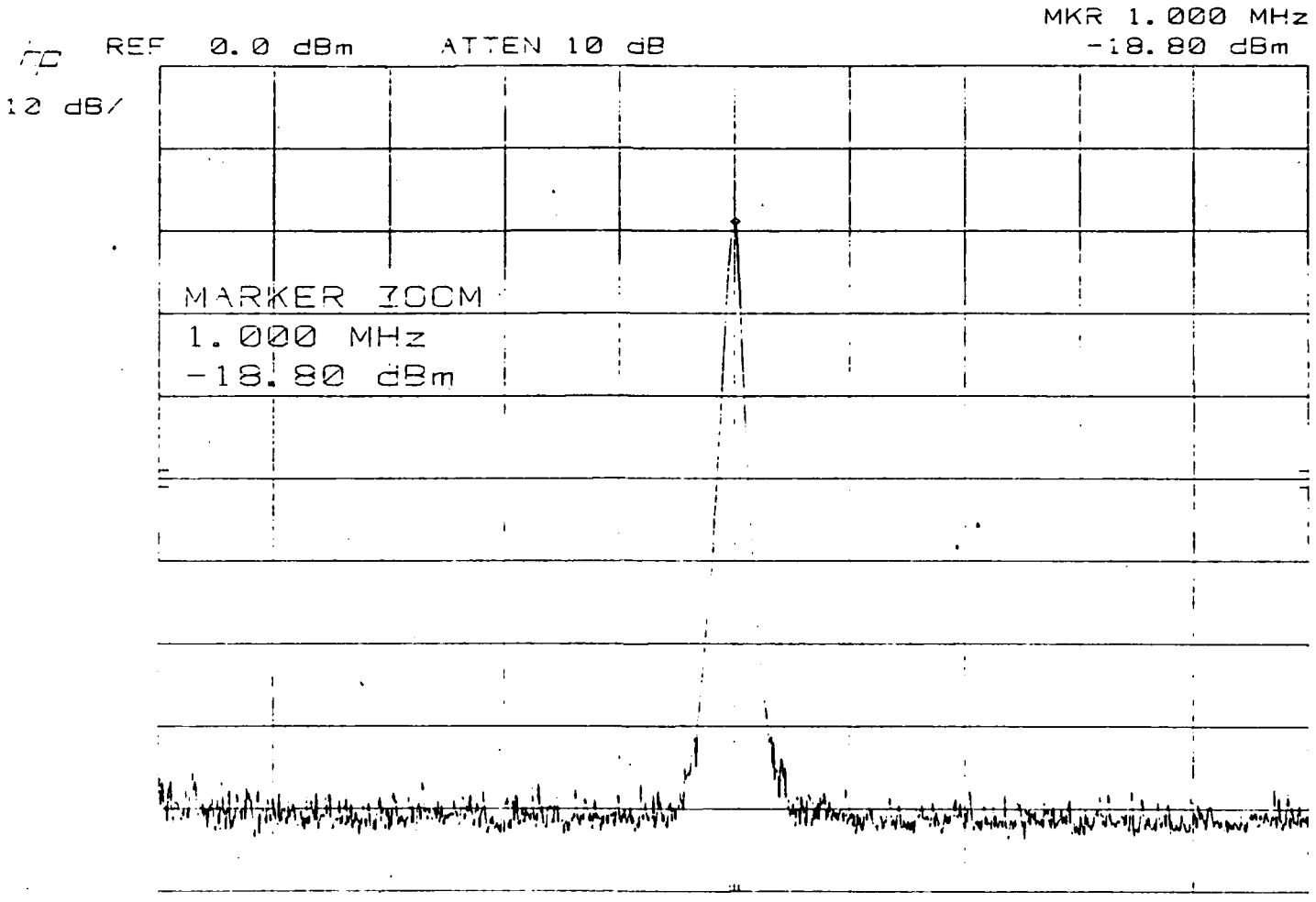
a high frequency on the unshielded receiver circuitry could be observed. A square waveform was chosen so that a spectral analysis could be accomplished and the resulting sinc pulse efficiently analyzed for center frequencies and power levels. A spectral analysis of the applied wave is shown in Figure 4.1. Figure 4.1 shows the spectrum of a sinc pulse with a power level of -18.80 dbm at a center frequency of 1 MHz (as indicated by the annotation to the left of the spectral peak).

Figure 4.2 shows the measured spectrum of the sinc pulse at a center frequency of 1 MHz with a power level of -79.10 dbm on the other receiver. This power represents the crosstalk due to the circuitry of the transmitter. In this observation the receiver circuitry was unshielded from the transmitter.

Figure 4.3 shows a sinc pulse spectrum at a center frequency of 1.0 MHz at a level of -81.30 dbm. This represents the amount of crosstalk that results with the receiver circuitry shielded from the transmitter. Thus the shielding provided an additional isolation of 2.2 db.

Figure 4.4 shows a sinc pulse at a center frequency of 1.00 MHZ at a level of -77.30 dbm. This is the crosstalk due to both the transmitting circuitry and CAF, mounted on the fiber optic module. In this case the receiver circuitry was left unshielded.

Figure 4.5 shows a sinc pulse at a center frequency of 1.00 MHz at a level of -78.50 dbm. This the crosstalk level due to both the transmitter and the CAF, but this time the



CENTER 1.00 MHz SPAN 1.81 MHz

RES BW 10 KHz VBW 30 KHz SWP 54.4 SEC

Figure 4.1 Applied 1 MHz Signal

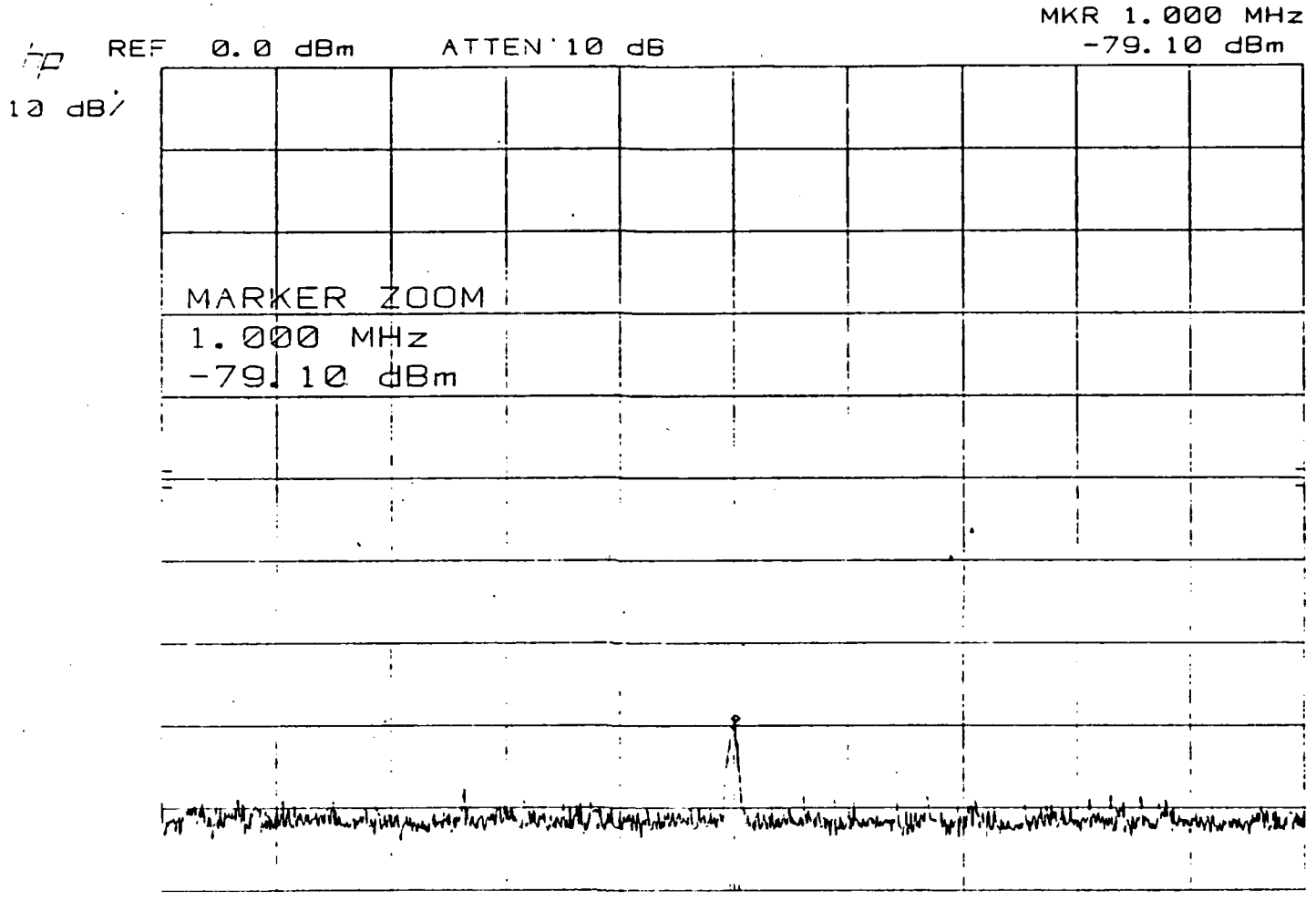


Figure 4.2 Unshielded Circuitry - Crosstalk

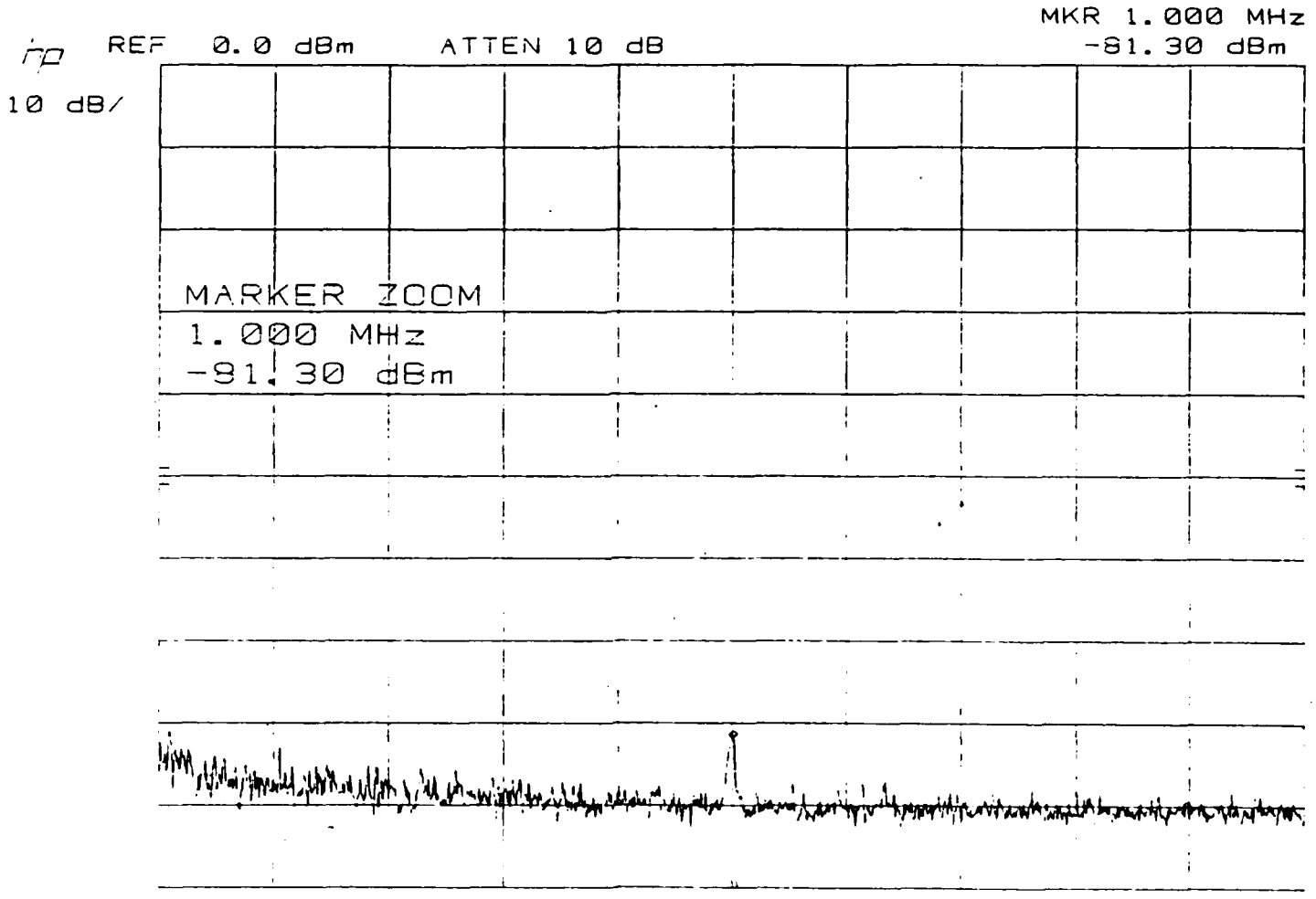


Figure 4.3 Shielded Circuitry - Crosstalk

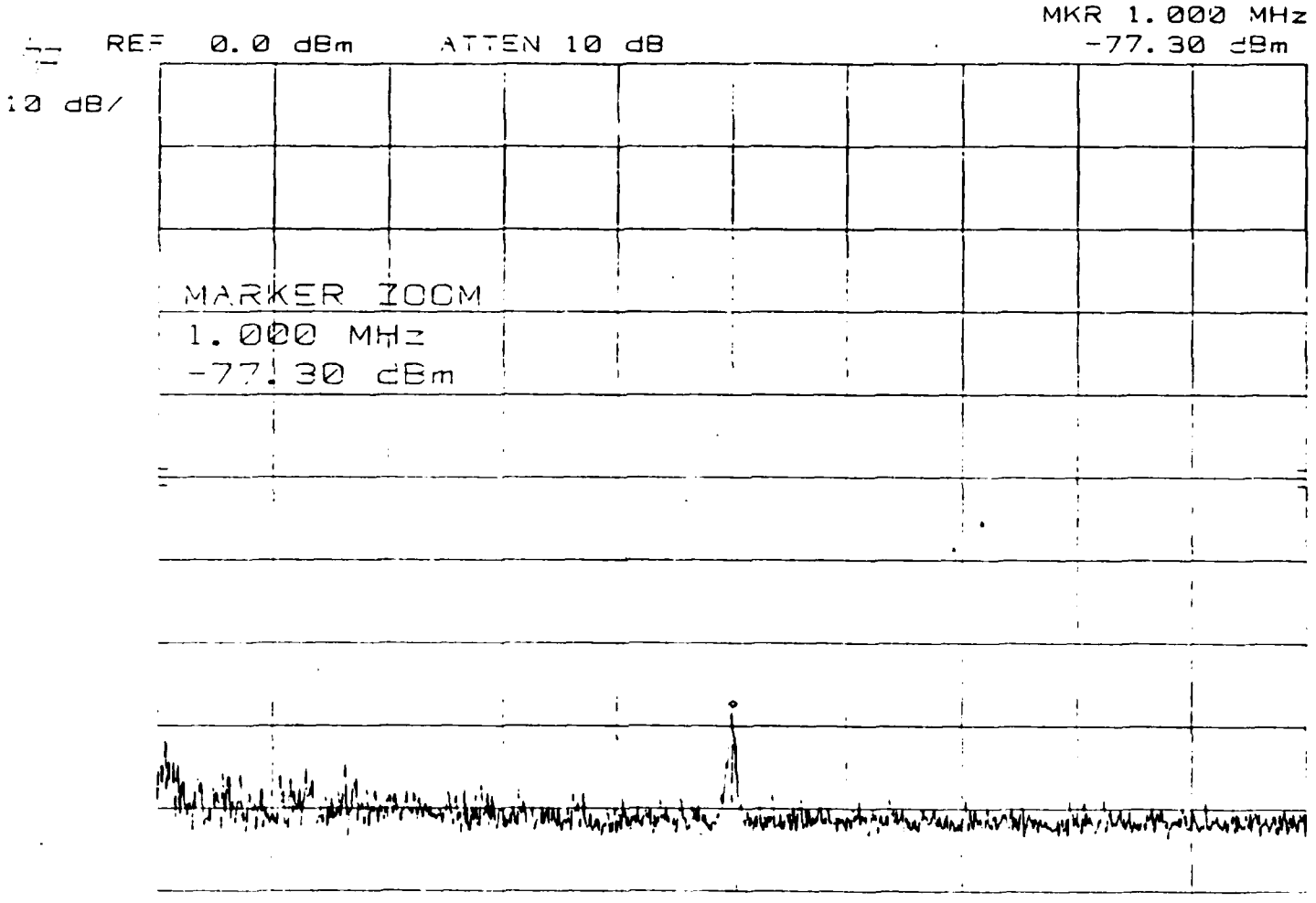


Figure 4.4 Unshielded Circuitry With CAF - Crosstalk

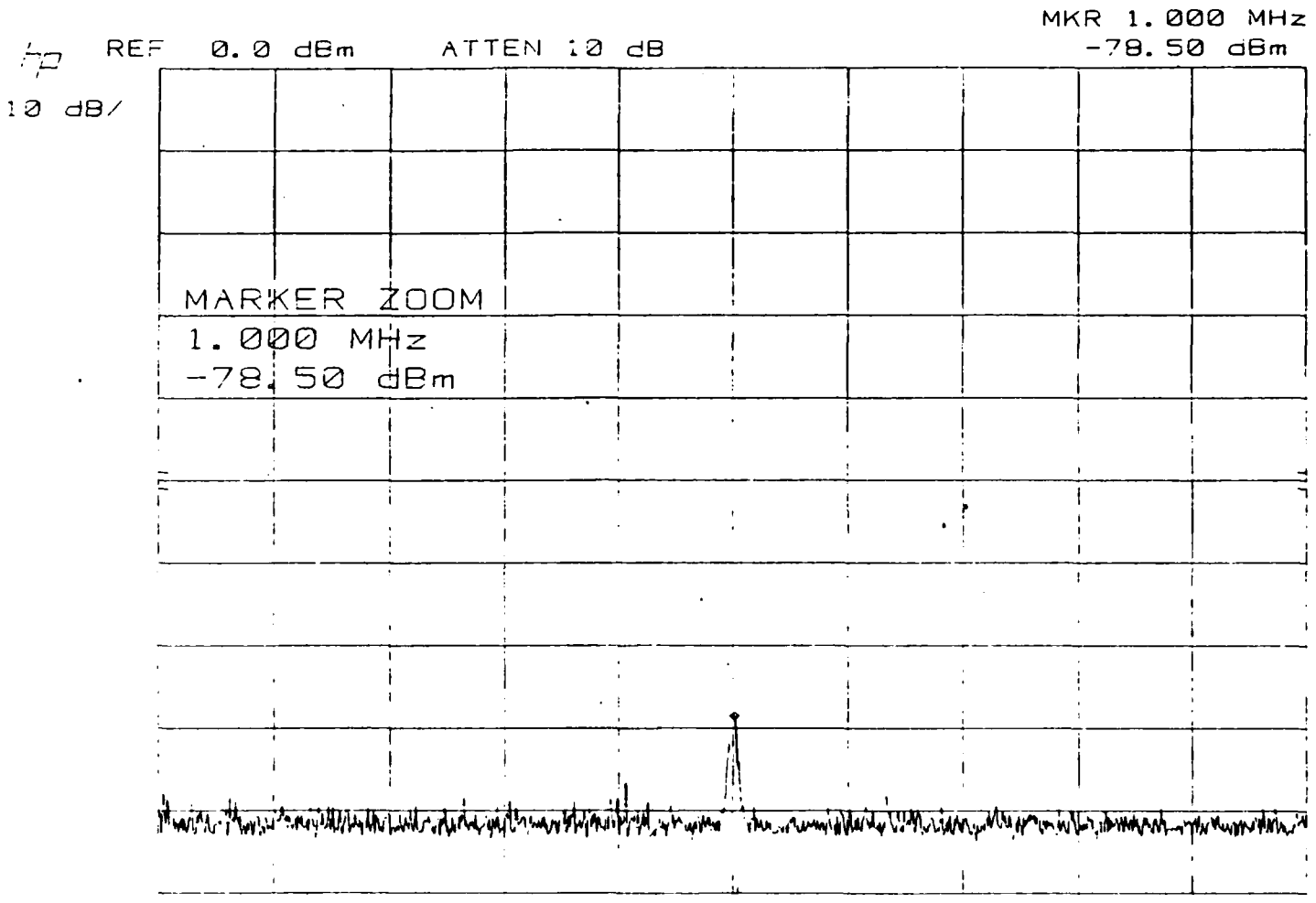


Figure 4.5 Shielded Circuitry With CAF - Crosstalk

receiver was shielded. The shielding gave an additional isolation of 1.2 db.

The object of these measurements was to observe the crosstalk due to the electronic emissions of the transmitter and the optical crosstalk of the CAF. Overall the CAF was observed to increase the crosstalk levels 1.2 to 2.8 db. This crosstalk is possibly due to internal reflections of light within the CAF being received by the PIN detector.

Although crosstalk is present in the system the levels present at would not be sufficient to cause an erroneous response from the receiver.

E. TRANSMITTED AND RECEIVED SIGNALS

The transmitted and received signals of the HP85 NEC configuration are shown in Figure 4.6. This diagram was obtained was obtained by using the Hewlett-Packard 1615A Logic Analyzer. Channel 0 shows the transmitted break signal from the NEC (refer to section A of chapter 3), while channel 1 shows the received break signal on the fiber optic module, channel 6 shows the transmitted data from the HP85 while channel 7 shows the data received at the end of the fiber. The distance of transmission was 1.27 kilometers on 50/125 micrometer fiber. It is noted that the HP85 is triggered on the trailing edge of the break signal.

In Figure 4.7 we see the data transmission of the HP85-AMPEX configuration. Channel 6 shows the transmitted data from

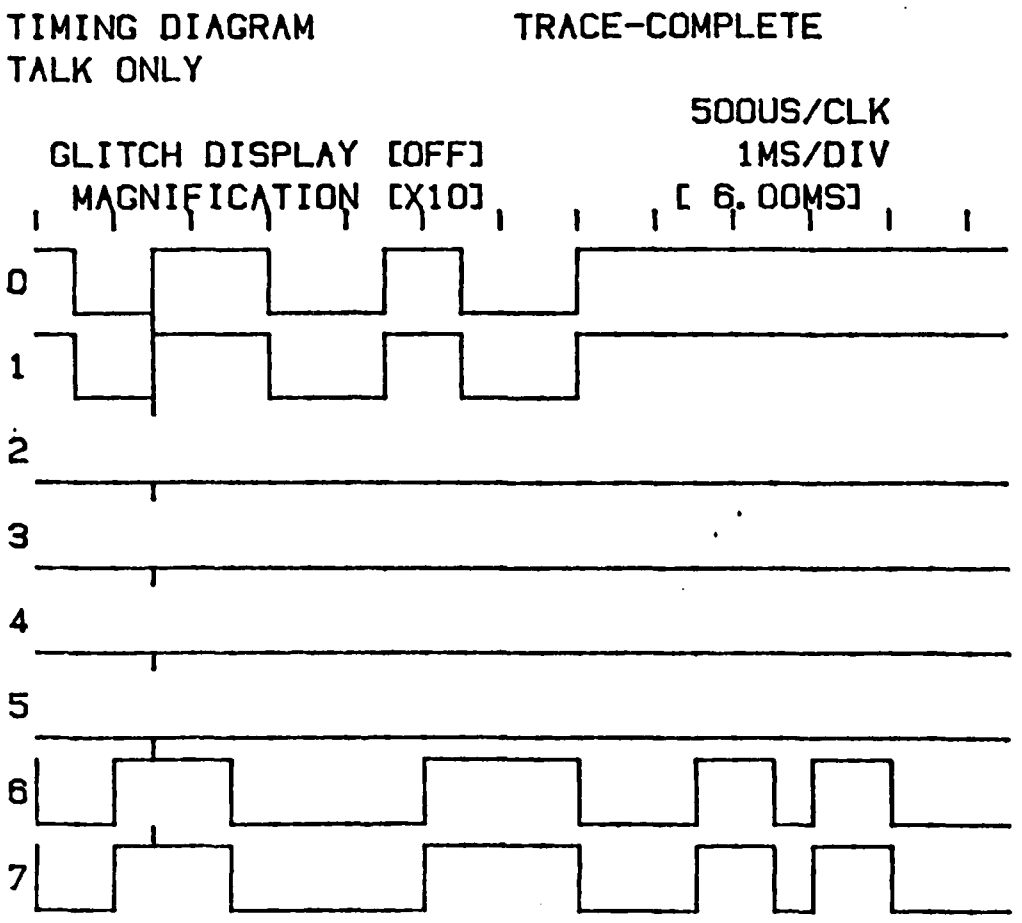


Figure 4.6 HP-85 NEC Signals

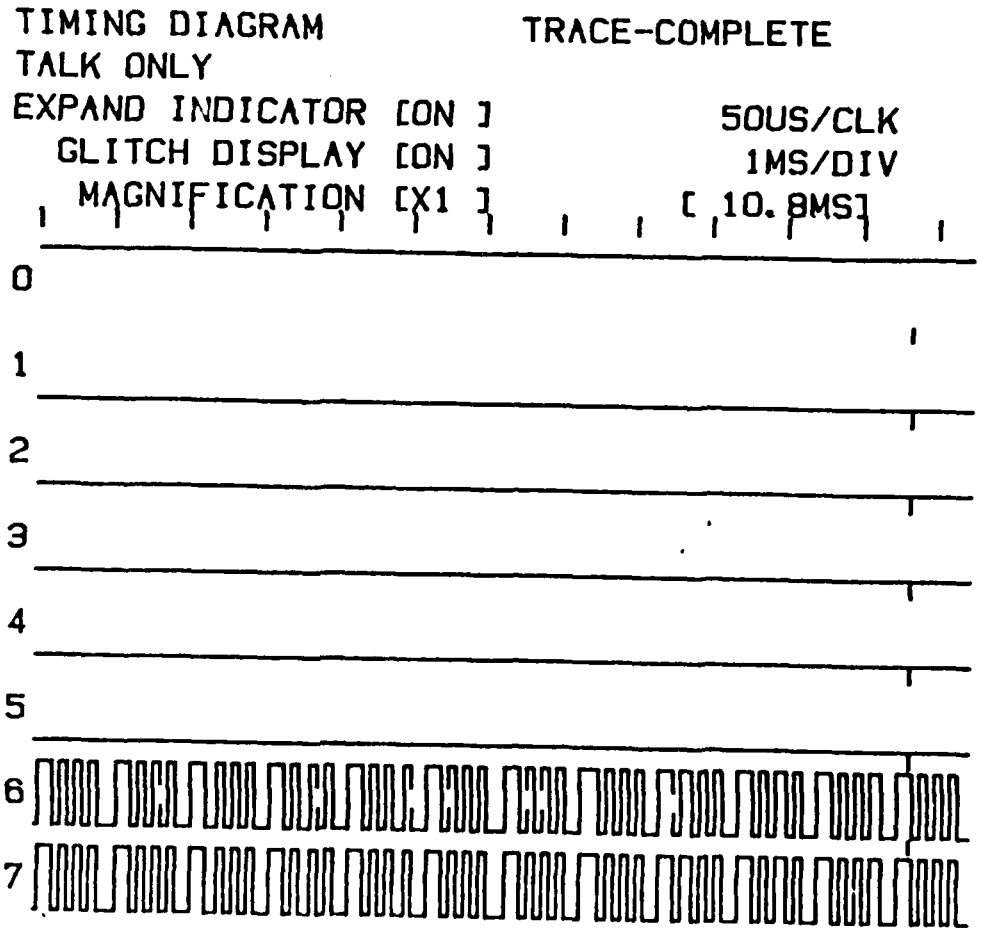


Figure 4.7 HP-85 AMPEX Signals

HP85 and channel 7 shows the received signal after the 1.27 kilometers link.

Signals of various frequencies were applied to the fiber optic modules to obtain the frequency range of the modules. The input frequencies ranged from 1 Hz to 5 MHz. Again the waveforms were chosen to be square waves so that a spectral analysis would be easy accomplished. Two different fibers were used to determine the losses due to the connectors and to observe the minimum sensitivity level of the detector. The frequencies and amplitudes observed are listed in Table V. Measurements were made of the amplitudes of the signal at the input to the fiber optic modules and after transmission on 3 meters of 50/125 micrometer graded index fiber to calculate the connector losses. On the average, depending on the orientation of the fiber, a connector loss of 1.25 dbm was observed. Transmission on the 1511 meters length of 100/140 micrometer fiber was performed as the author believes that this would be a realistic distance necessary for a high speed data link. From Table V it is seen that at 5 MHz the maximum sensitivity of the PIN detector is reached (-44.0 dbm). A spectral analysis of the signals listed in Table V are shown in Figures 4.8 to 4.25. Explanation of these figures follows.

Figure 4.8 shows the spectral analysis and power level of a 1 Hz square wave that was applied to the input of the fiber optic modules. As seen in Figure 4.8 the spectral analysis the waveform is a sinc shape at a center frequency of 1 Hz with a

TABLE V

APPLIED AND RECEIVED SIGNALS

FREQUENCY	INPUT SIGNAL (dbm)	REC. SIGNAL 3M F.O CABLE (50/125 um) (dbm)	REC. SIGNAL 1511M CABLE (100/140 um) (dbm)
1 HZ	-6.90	-9.60	-10.30
100 HZ	-17.80	-20.60	-36.70
1 KHZ	-18.50	-20.50	-35.90
10 KHZ	-17.80	-20.50	-35.60
1 MHZ	-18.40	-21.00	-37.60
5 MHZ	-19.80	-21.80	-44.00

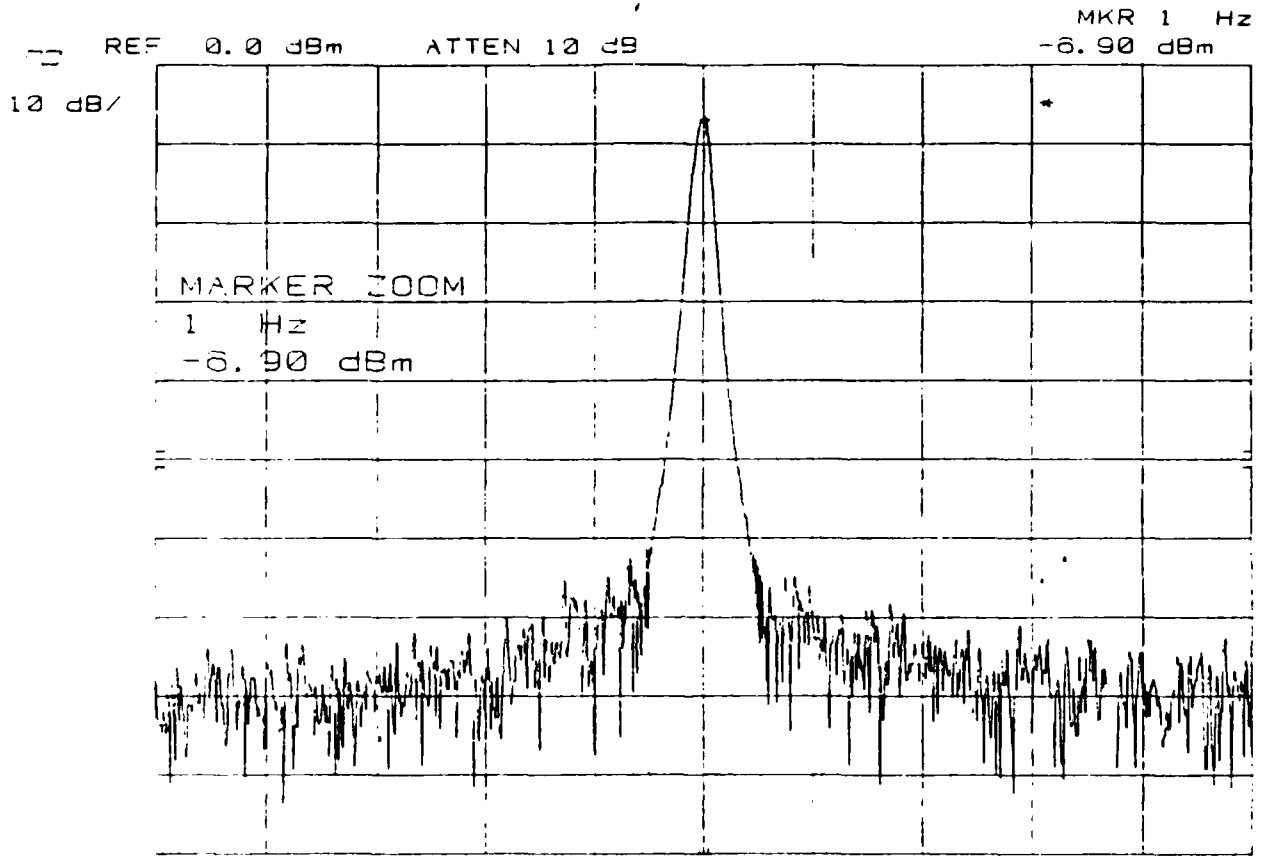


Figure 4.8 1 Hz Applied Signal

power level of -6.90 dbm. A 1 Hz signal was applied to ensure that the modules would be able to respond to the lowest frequency seen experimentally for two DTEs, without experiencing significant delay or distortion on a long distance link.

Figure 4.9 shows the same sinc spectrum after 3 meters of fiber. The level of power is observed to -9.60 dbm. Since 3 meters of fiber has a negligible amount of attenuation at 7 db/km the losses seen here are attributed to connectors. Here a total connector loss of 2.7 db is seen.

Figure 4.10 shows the 1 Hz sinc spectrum after transversing the 1511 meter fiber. A signal with a center frequency of 1 Hz is observed at a level of -10.30 dbm. This power level is more than sufficient to trigger a response from the receiver circuitry. Thus the link would be able to handle the lowest frequency transmitted by the DTEs.

Frequencies of 100 Hz, 1KHz, and 10 KHz were applied to the modules as these would be typical of the frequencies seen by the RS232.

Figure 4.11 shows the spectral analysis of 100 Hz square wave applied input signal. The sinc spectrum shown in Figure 4.11 has a center frequency of 100 Hz at a level of -17.80 dbm.

Figure 4.12 has the same sinc spectrum after the 3 meter fiber. This also has a center frequency of 100 Hz at a level of -20.60 dbm. This implies a total connector loss of 2.8 db.

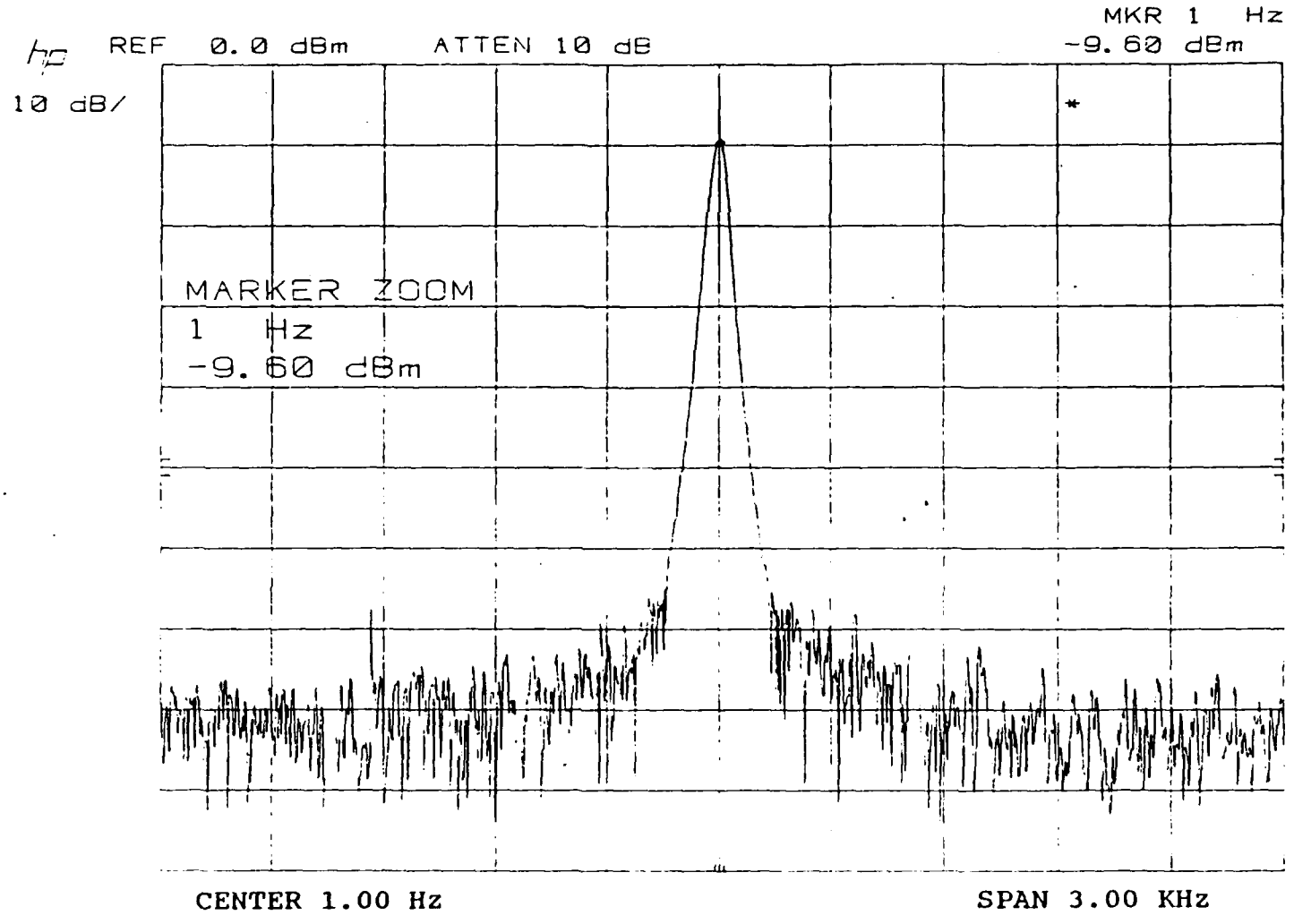


Figure 4.9 1 Hz Signal After 3 Meters

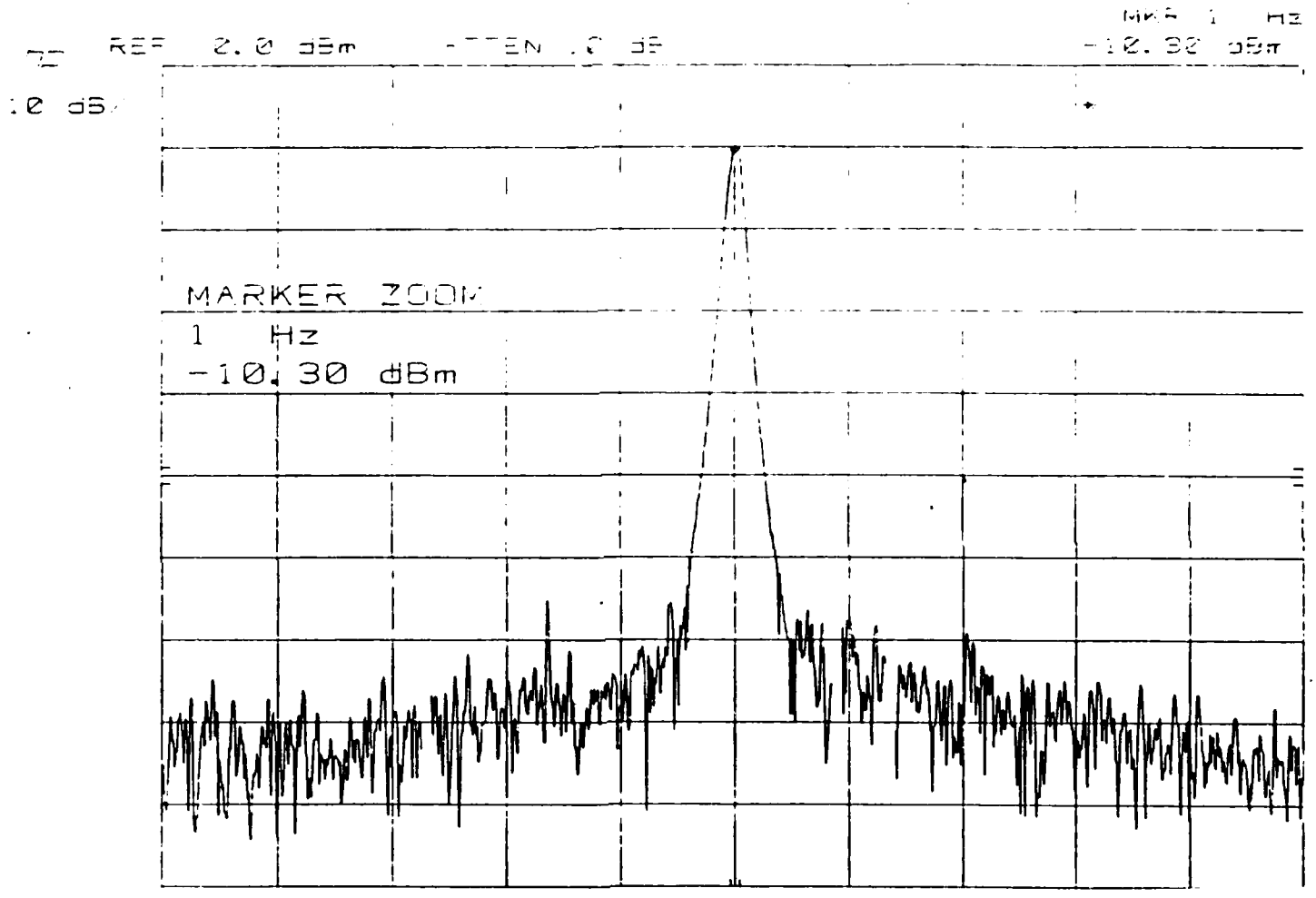


Figure 4.10 1 Hz Signal After 1511 Meters

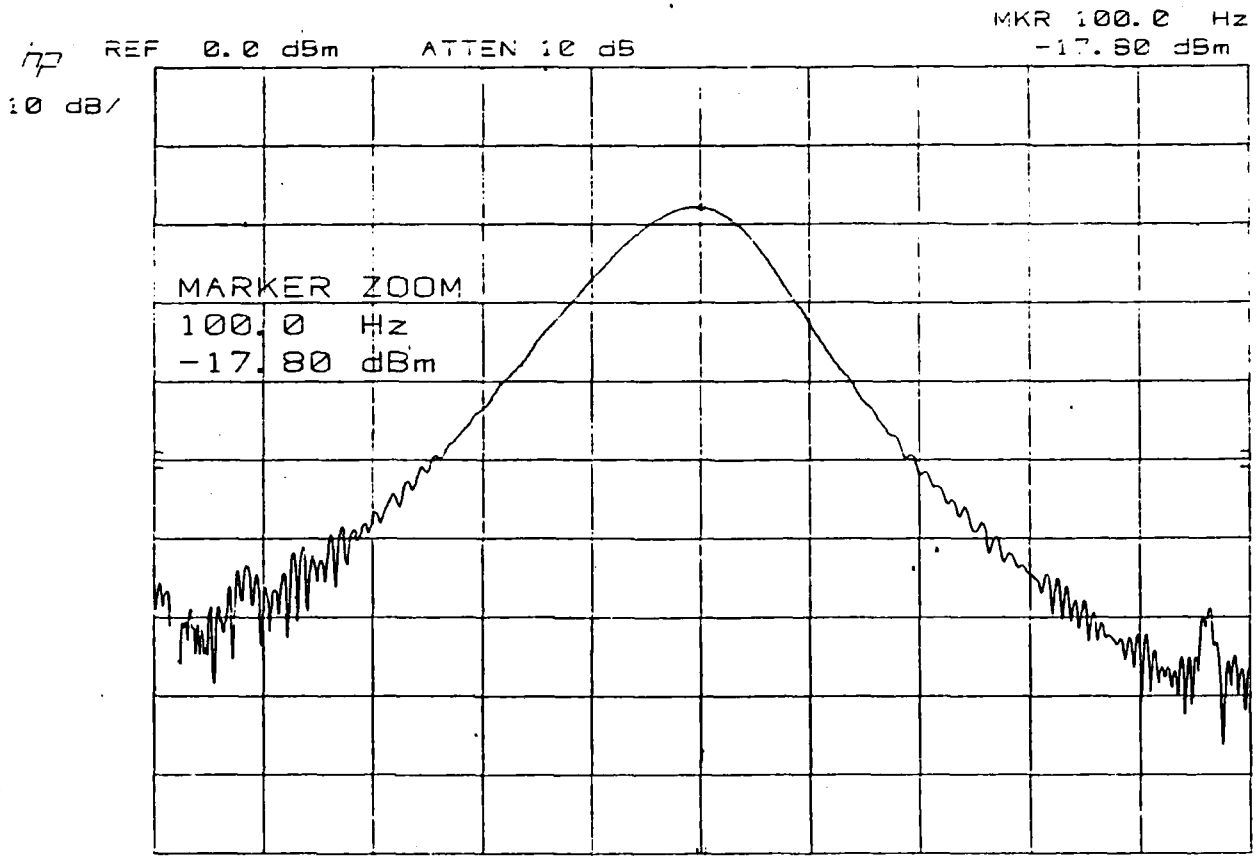


Figure 4.11 100 Hz Applied Signal

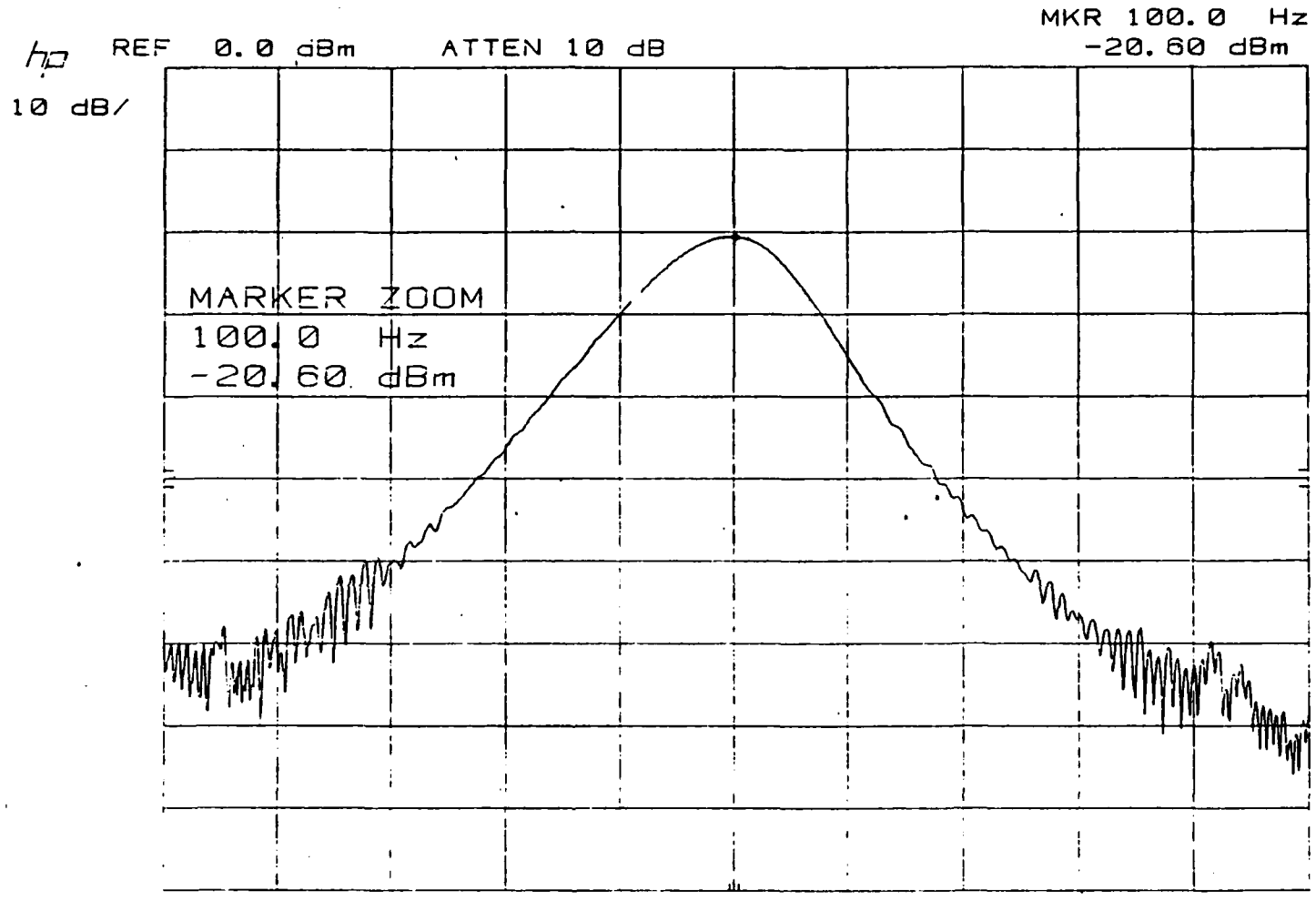


Figure 4.12 100 Hz Signal After 3 Meters

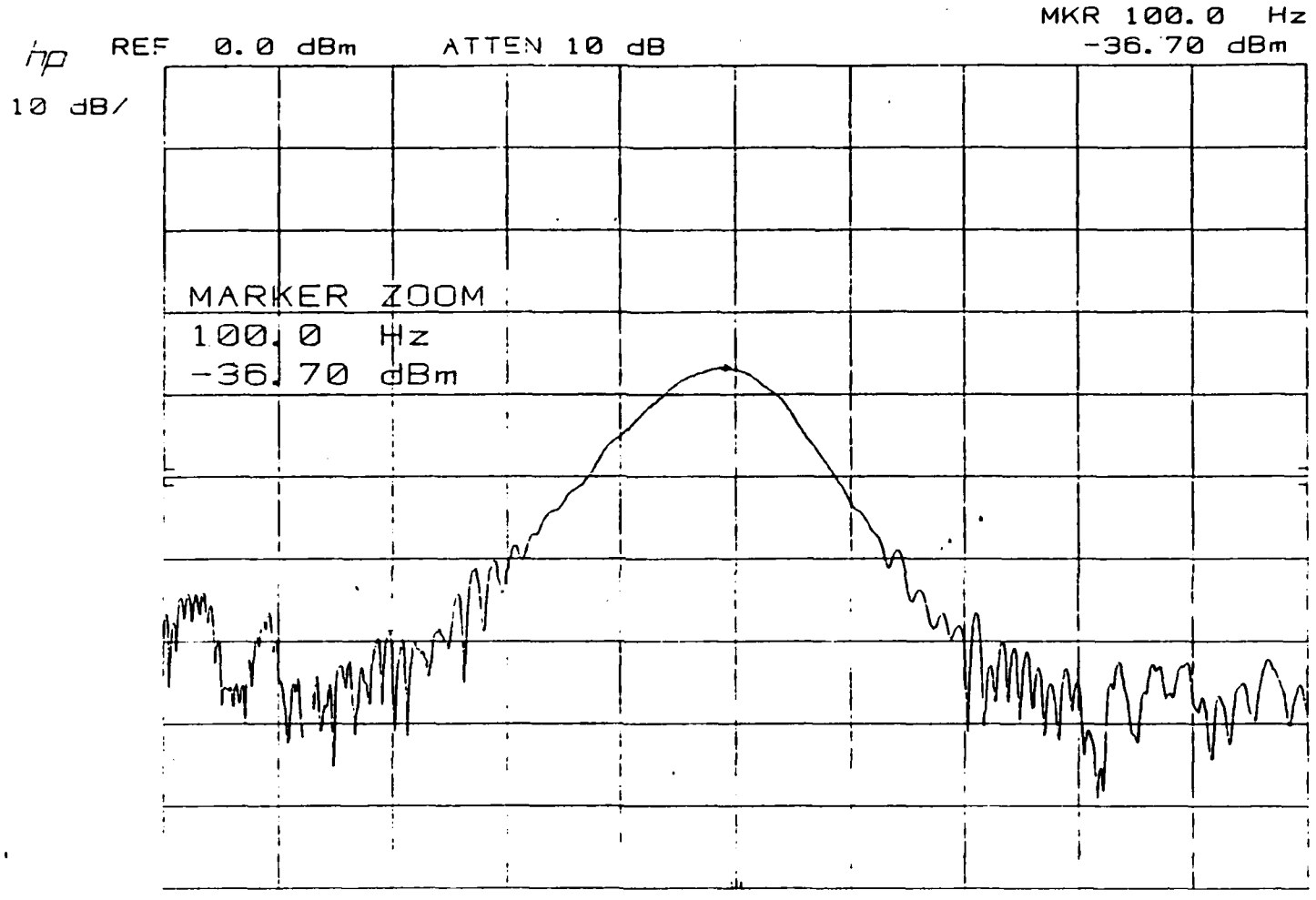
Figure 4.13 displays the 100 Hz spectrum after the 1511 meter fiber at a center frequency of 100 Hz and a power level of -36.70 dbm, well within the receiver sensitivity limit of -44.0 dbm.

In Figure 4.14 a spectral analysis of an applied 1 KHz square wave is shown. The resulting spectrum pulse has a frequency of 1 KHz at a power level of -18.50 dbm. This same signal is observed in Figure 4.15 after the 3 meter fiber, a power level of -20.50 dbm, to give a total connector loss of 2.0 db. This improved connector loss may have been the result of an improved orientation of the fiber to the connectors of the fiber optic modules.

Figure 4.16 displays the spectrum of the signal after the 1511 meters of fiber. A center frequency of 1.0007 KHz at a power level of -35.90 dbm, still within the limits of the receiver.

Figure 4.17 shows a spectral analysis of an applied square wave at 10 KHz. The figure shows a center frequency of 10 KHz at a power level of -17.80 dbm. Figure 4.18 has the spectrum after the 3 meter fiber to give a total connector loss of 2.7 db.

Signals of frequencies 1 MHz and 5 MHz were also applied to the fiber optic modules. These high frequencies were chosen as they would reflect a data flow that would be seen on a local area network.



CENTER 100 Hz SPAN 100 Hz

RES BW 10 Hz VBW 30 Hz SWP 3.00 SEC

Figure 4.13 100 Hz Signal After 1511 Meters

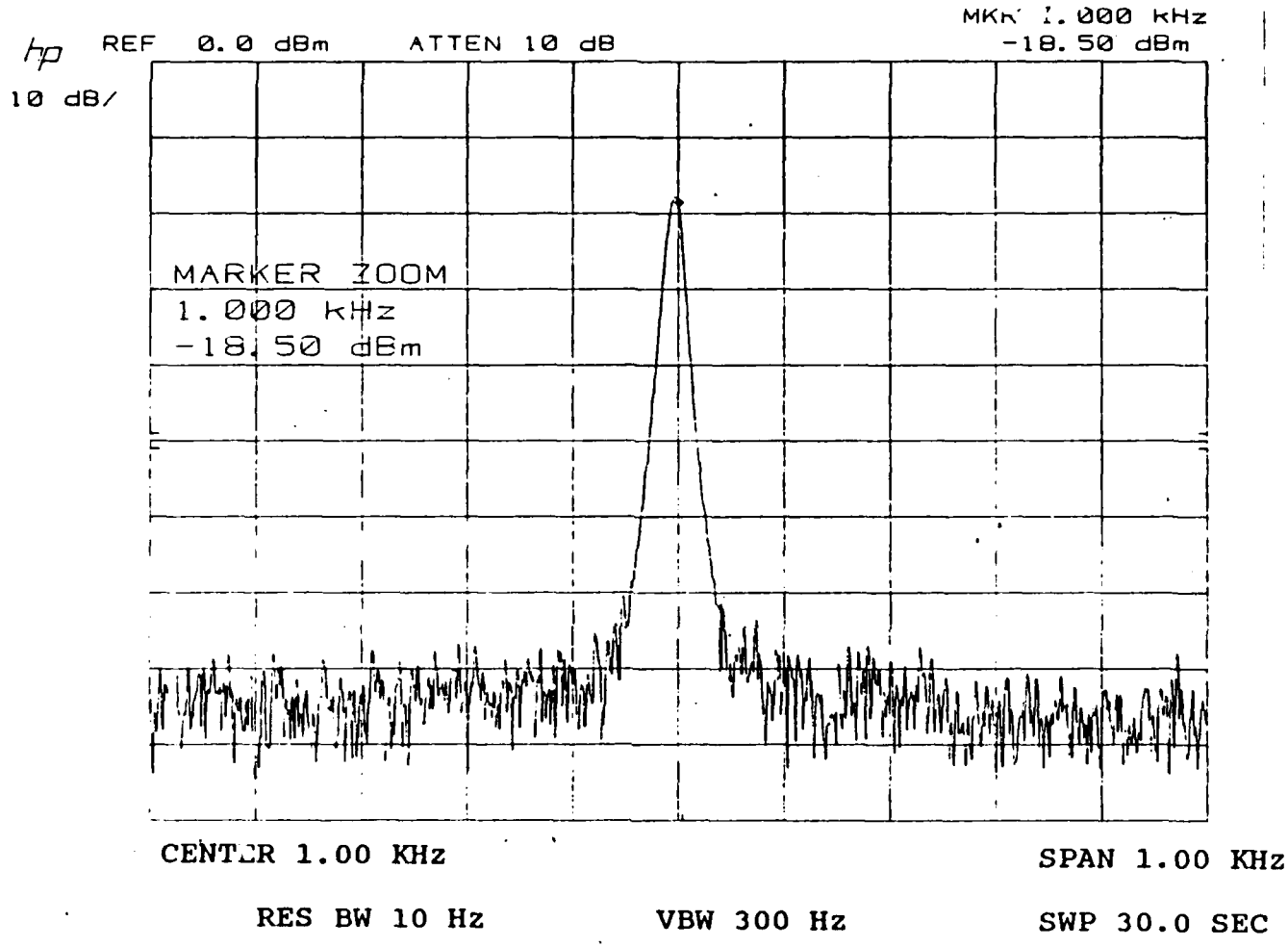


Figure 4.14 1 KHz Applied Signal

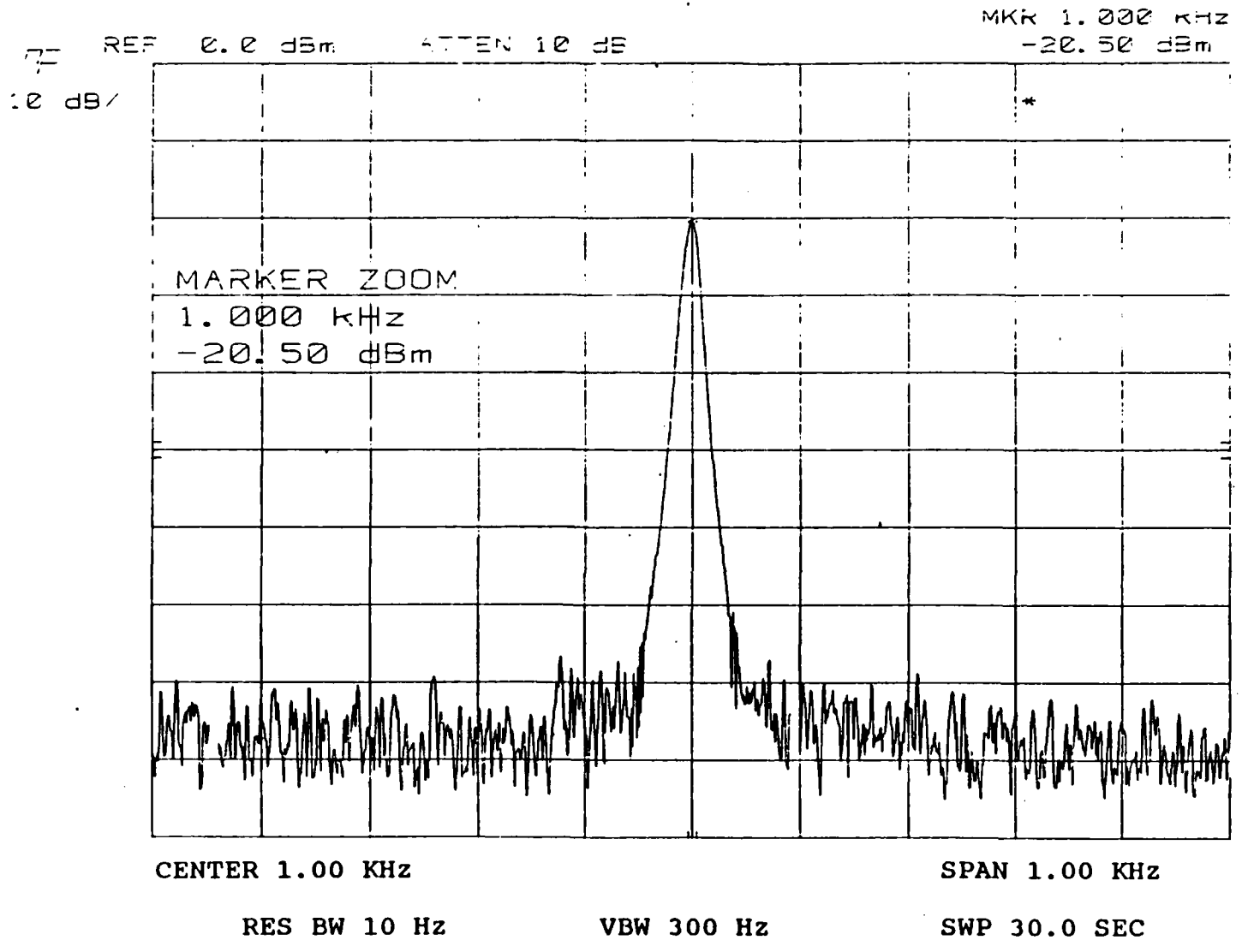


Figure 4.15 1 KHz Signal After 3 Meters

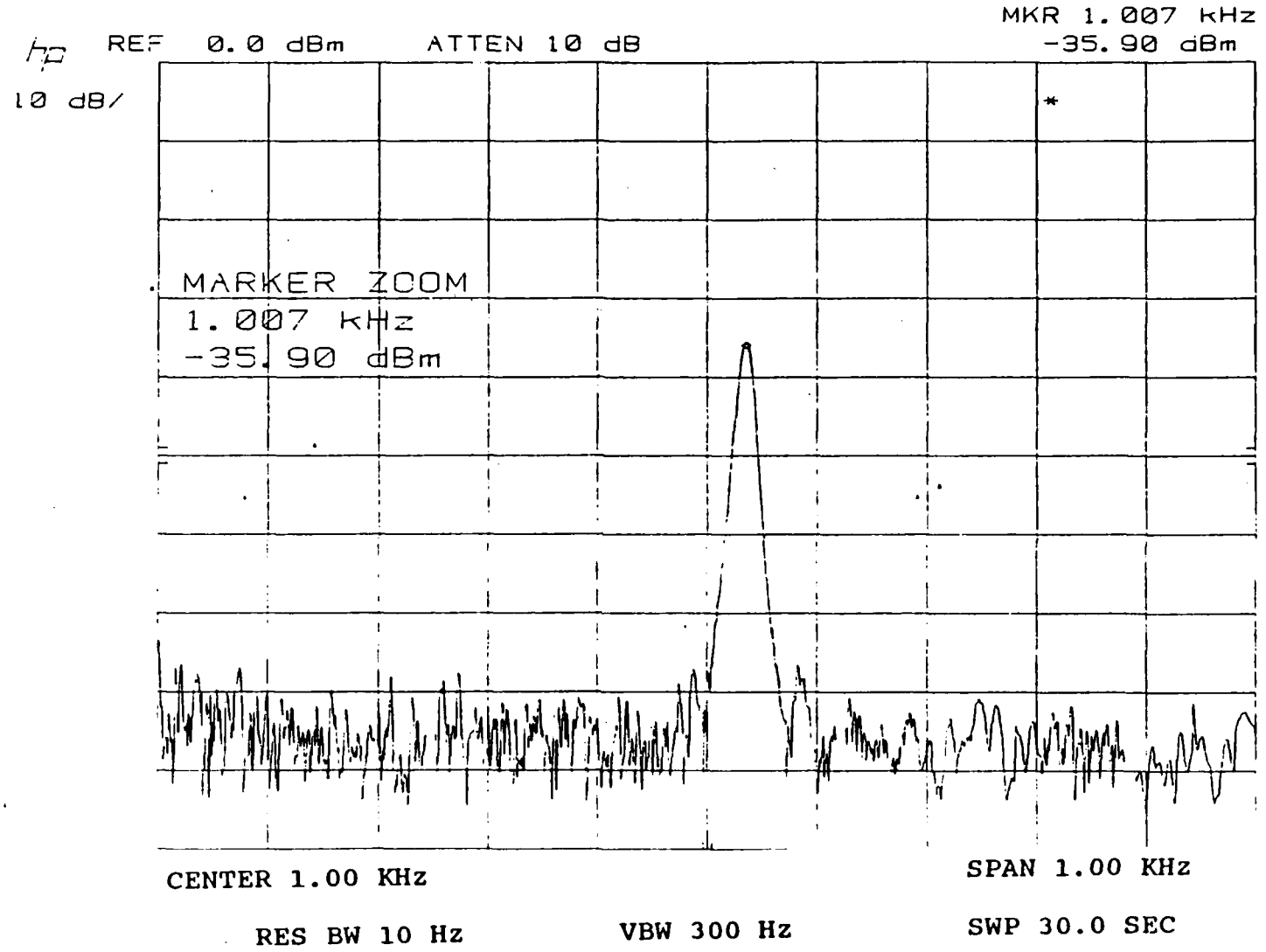


Figure 4.16 1 KHz Signal After 1511 Meters

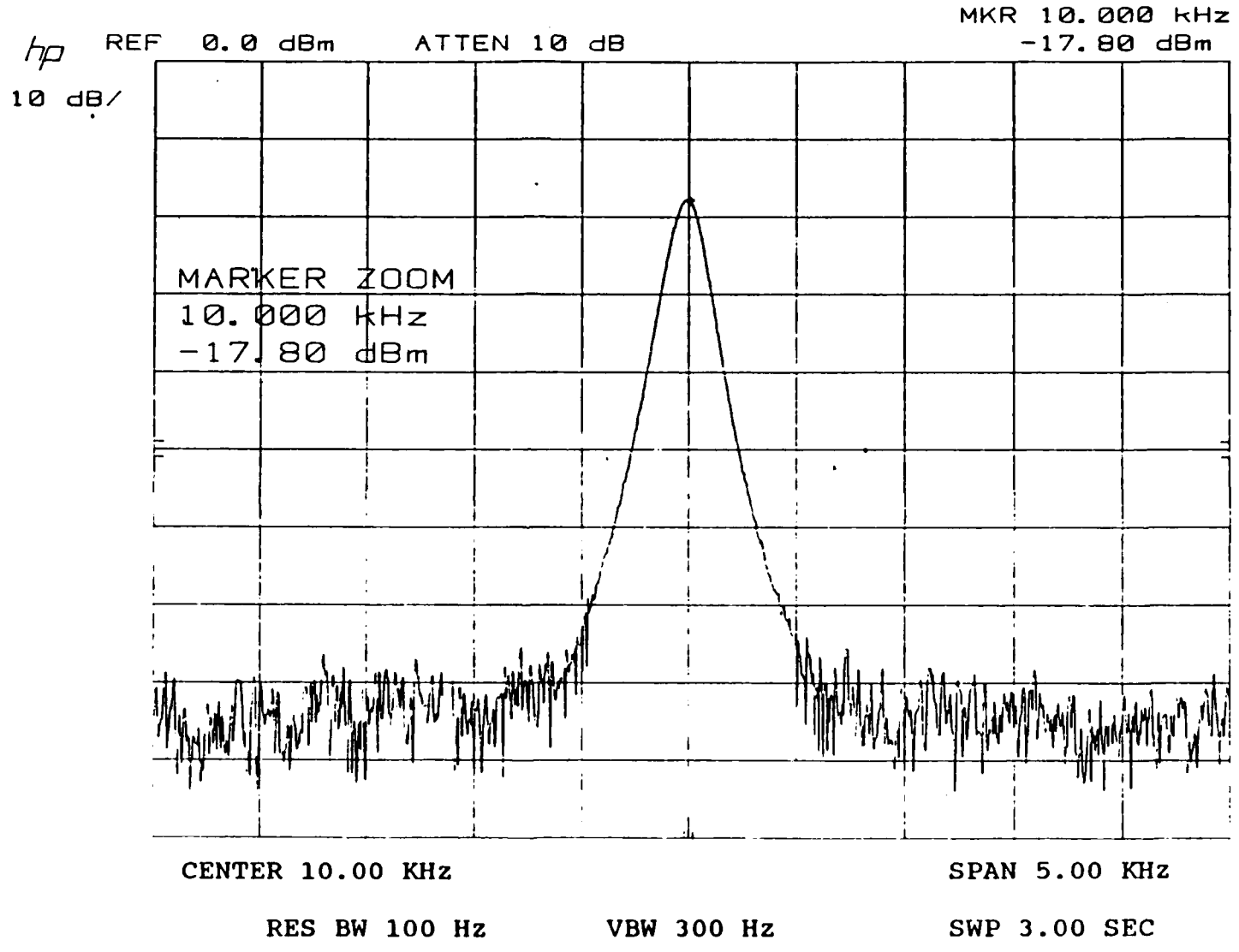


Figure 4.17 10 KHz Applied Signal

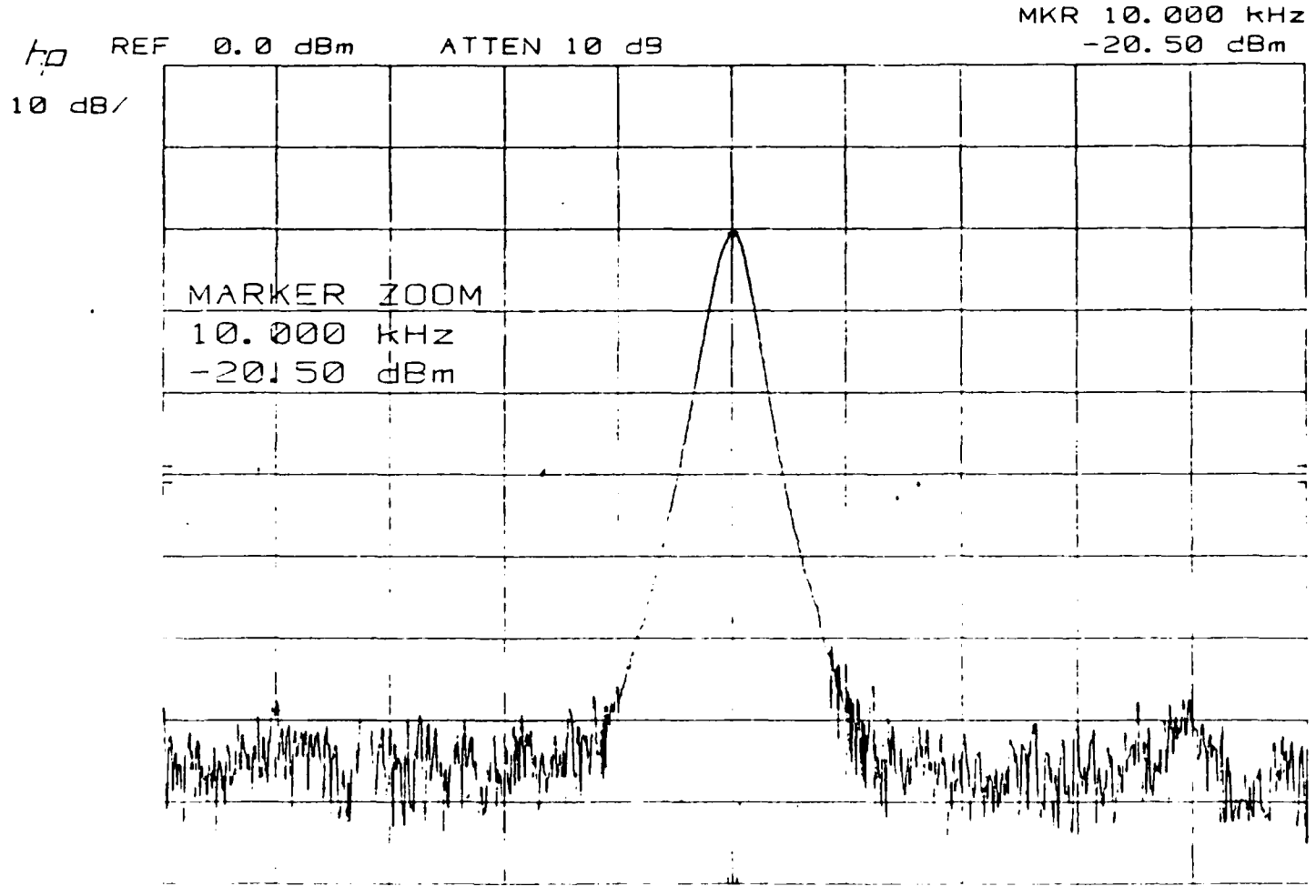


Figure 4.18 10 KHz Signal After 3 Meters

Figure 4.19 shows the same 10 KHz sinc spectrum after the 1511 meter fiber at an amplitude of -35.60 dbm, a level that would still trigger a response from the receiver circuitry.

Figure 4.20 shows a spectral analysis of an applied 1 MHz square wave with power level of -18.40 dbm. Figure 4.21 shows the signal after the 3 meter fiber at a level of -21.0 dbm, giving a total connector loss of 2.6 db.

Figure 4.22 displays the received sinc pulse after the 1511 meter fiber at a center frequency of 1 MHz and a power level of -37.60 dbm. This signal is 6.4 dbm above the threshold of the receiver circuitry.

Figure 4.23 shows the spectral analysis of the highest frequency that the fiber optic modules were able to discern, 5 MHz. This sinc pulse has an input amplitude of -19.80 dbm. Figure 4.24 has the same signal after the 3 meter fiber at a level of -21.80 dbm to give a total connector loss of 2.0 db.

Figure 4.25 shows the received sinc pulse after 1511 meters of fiber. The center frequency is still at 5 MHz, however, the power level of the signal is seen to be at the maximum sensitivity level of the receiver, -44.0 dbm.

The fiber optic modules frequency range is effectively from d.c. to 5 MHz, an increase of 250 times that of the bandwidth of the RS232. The capability of the modules to handle 1 to 5 MHz signals opens the system up to the possibility of being utilized on a local area network.

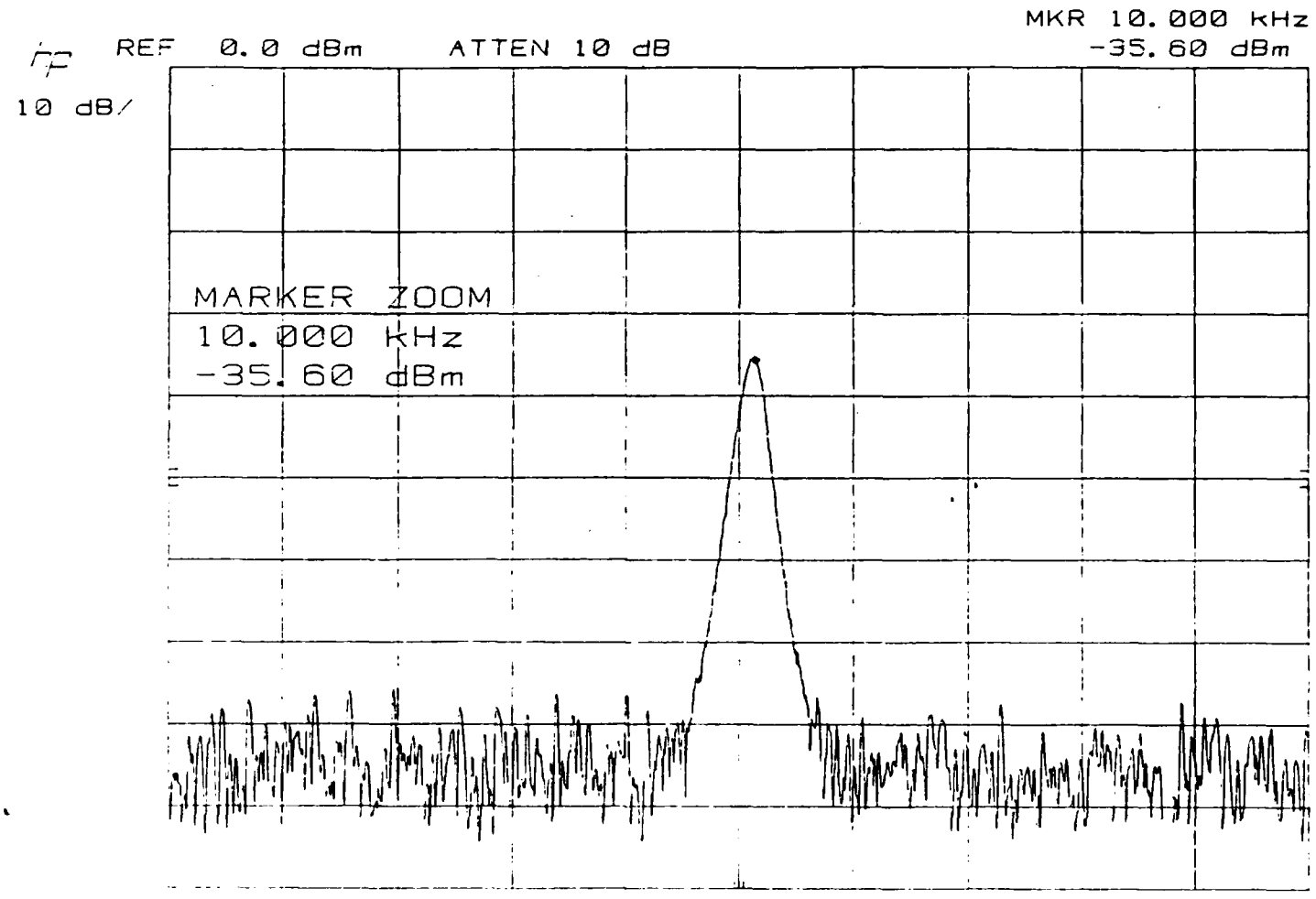


Figure 4.19 10 KHz Signal After 1511 Meters

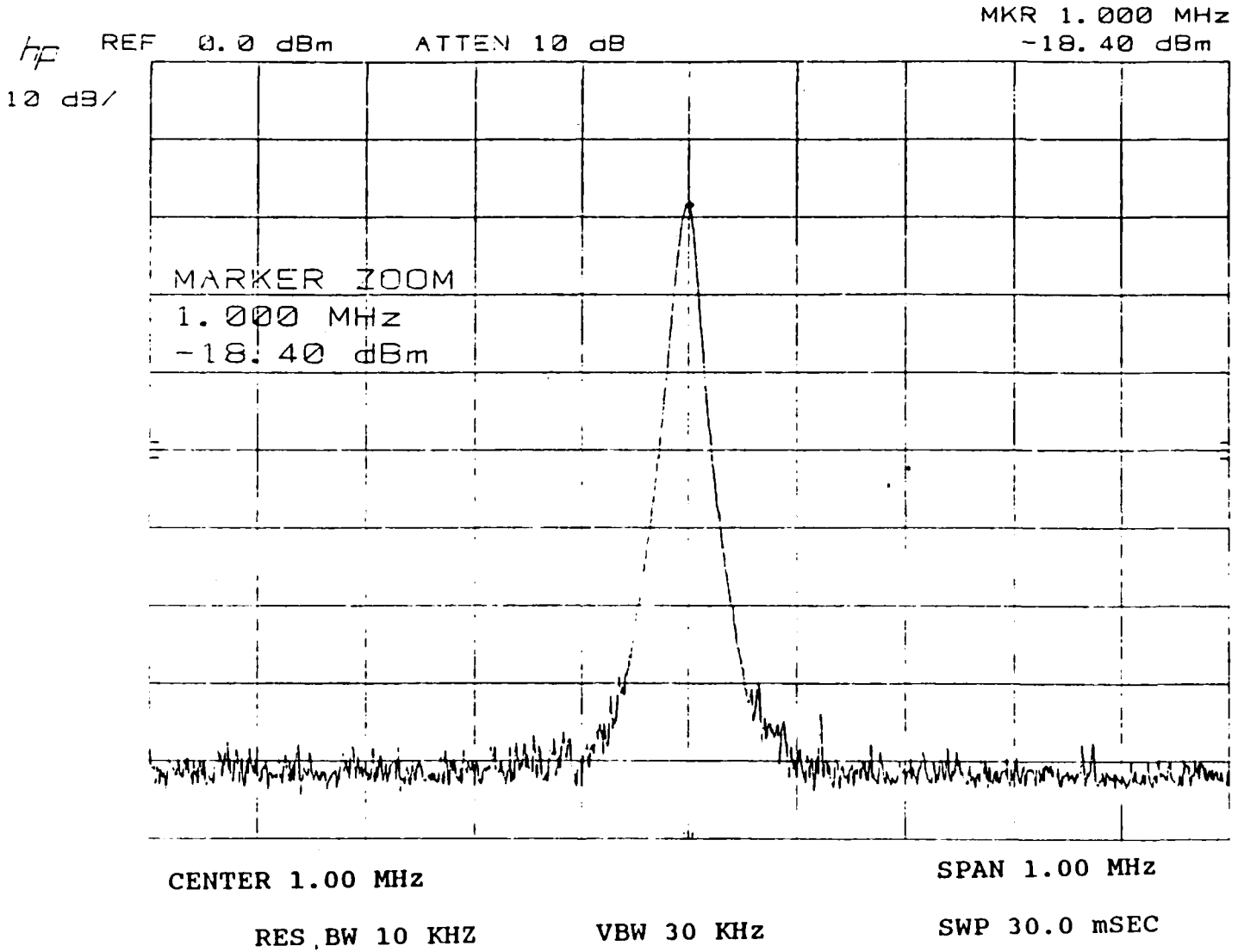


Figure 4.20 1 MHz Applied Signal

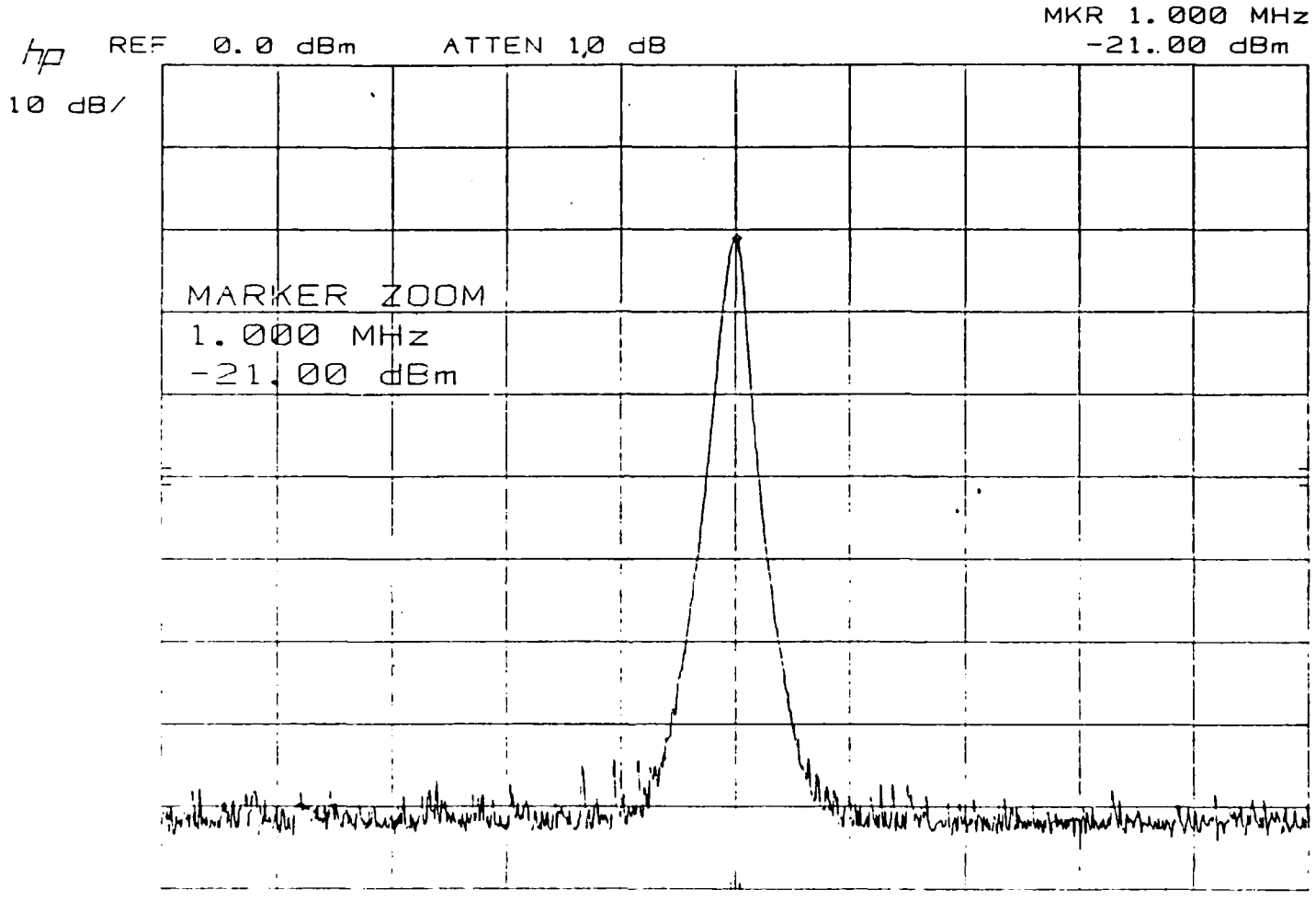


Figure 4.21 1 MHz Signal After 3 Meters

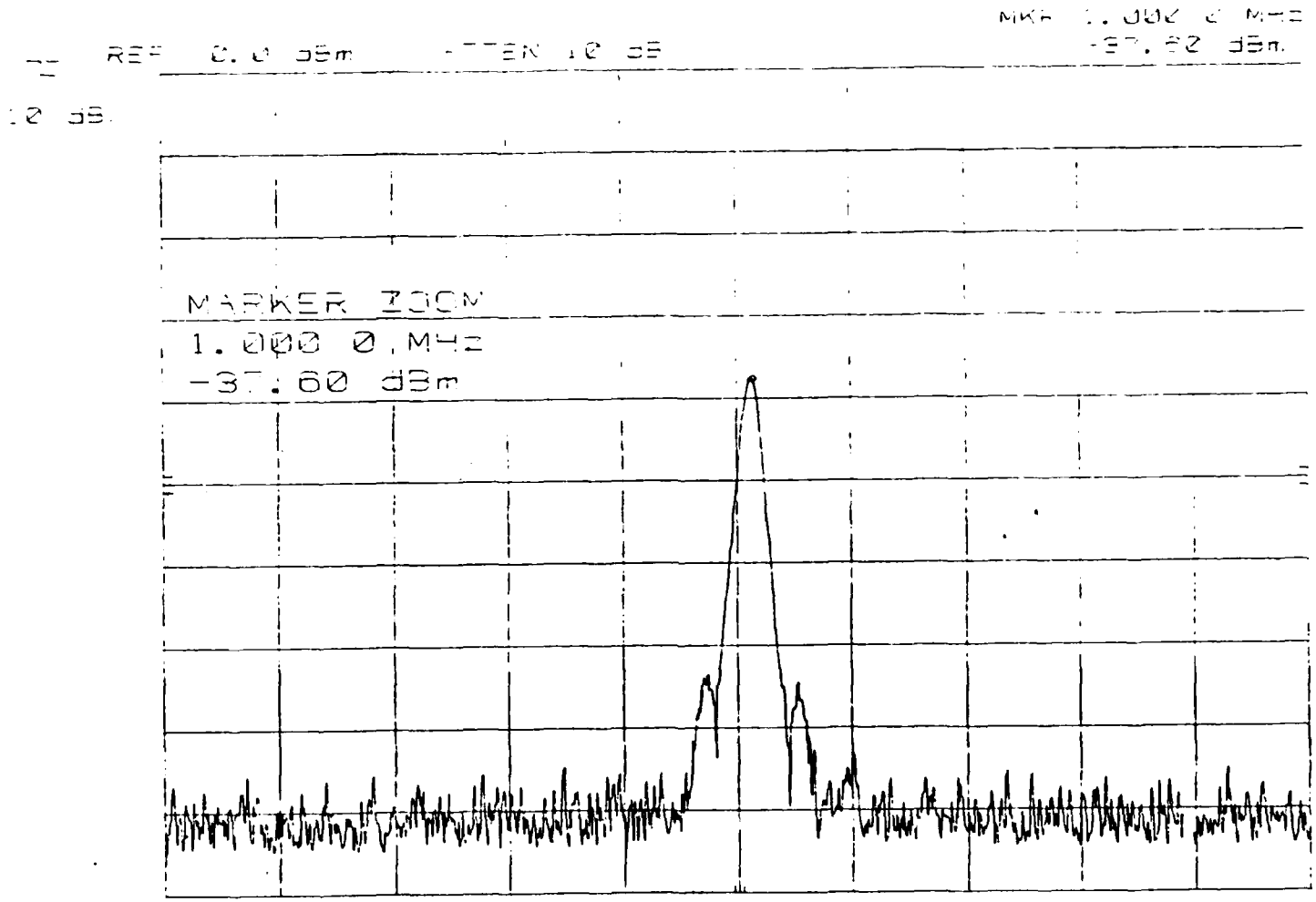


Figure 4.22 1 MHz Signal After 1511 Meters

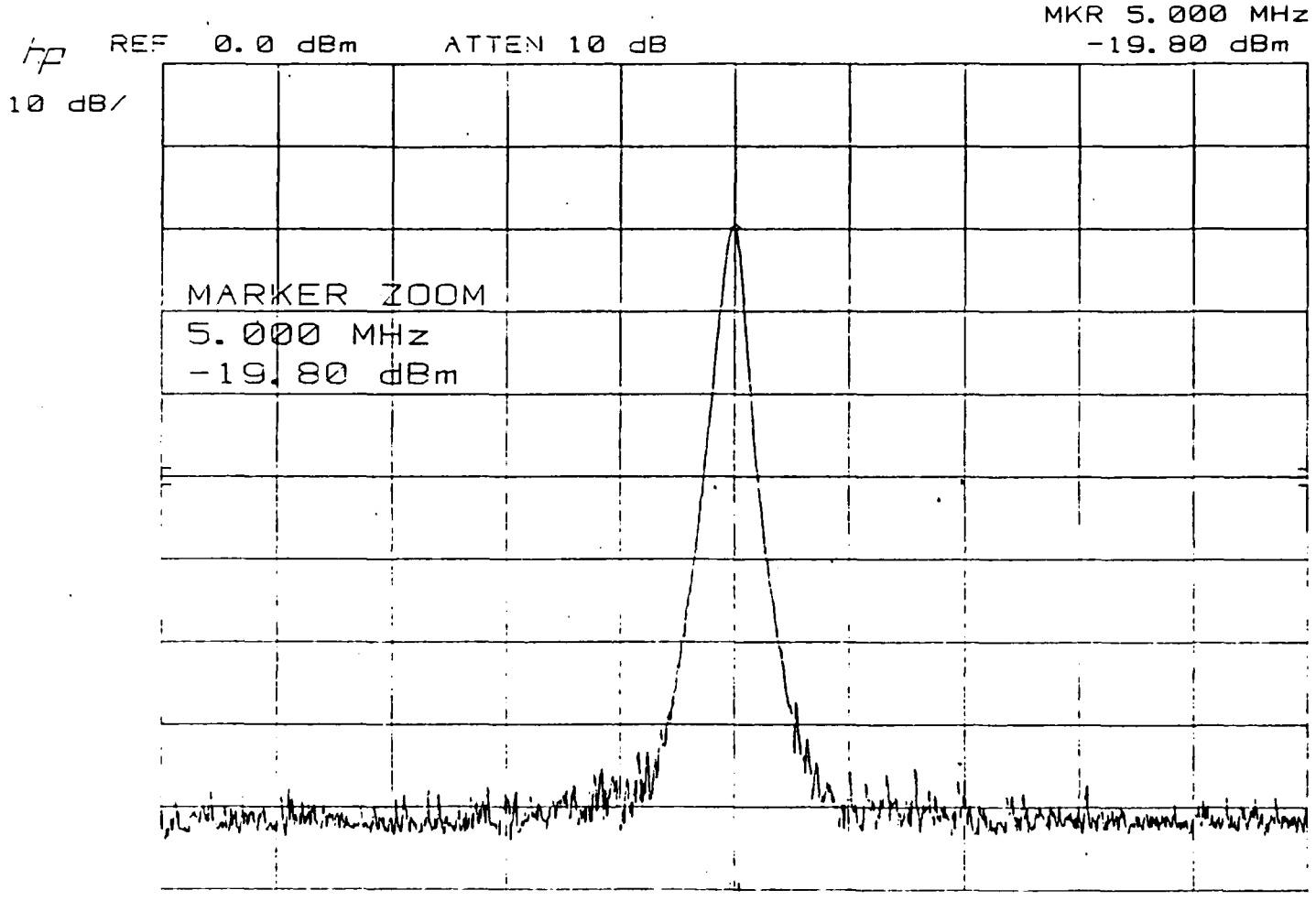


Figure 4.23 5 MHz Applied Signal

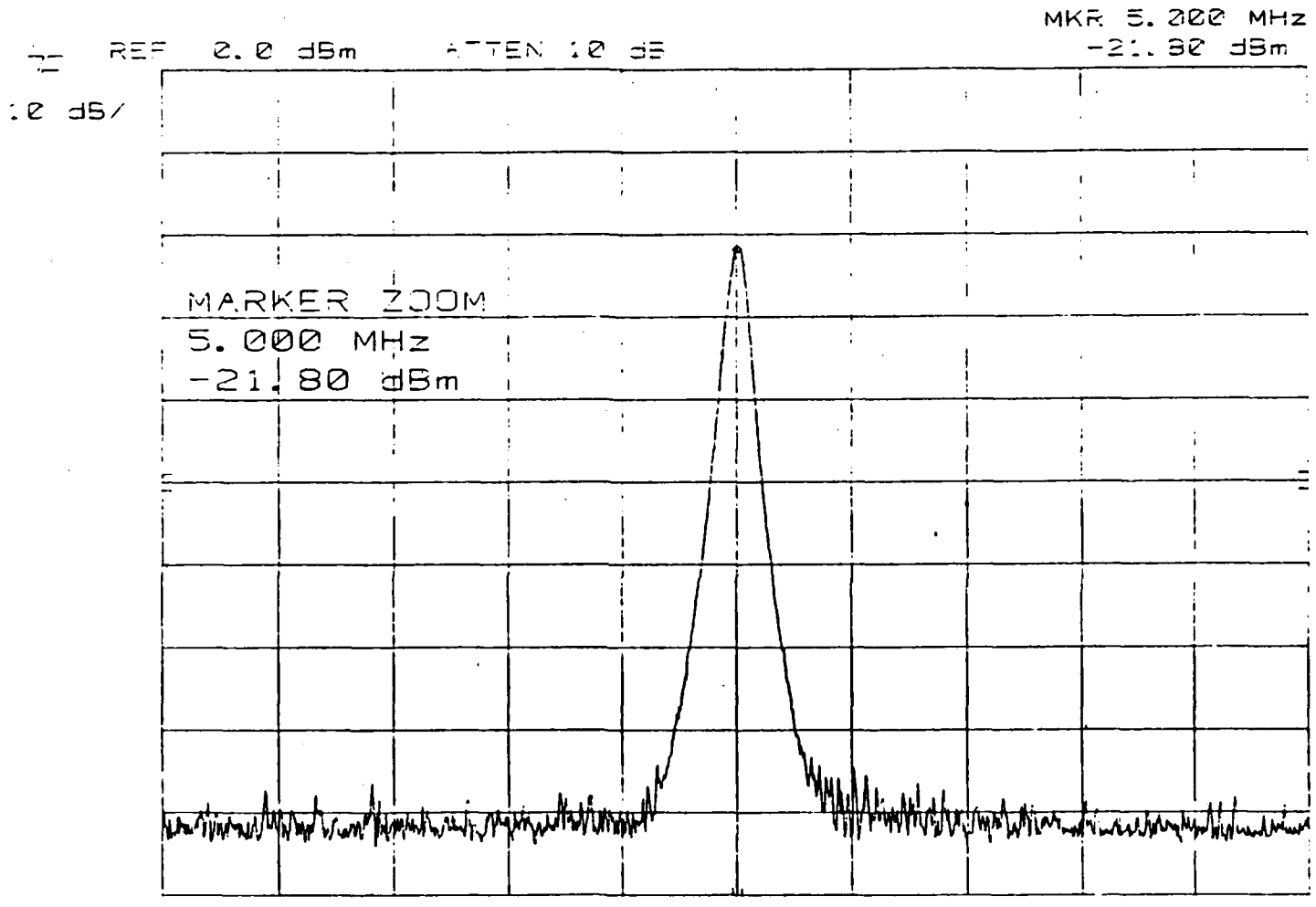


Figure 4.24 5 MHz Signal After 3 Meters

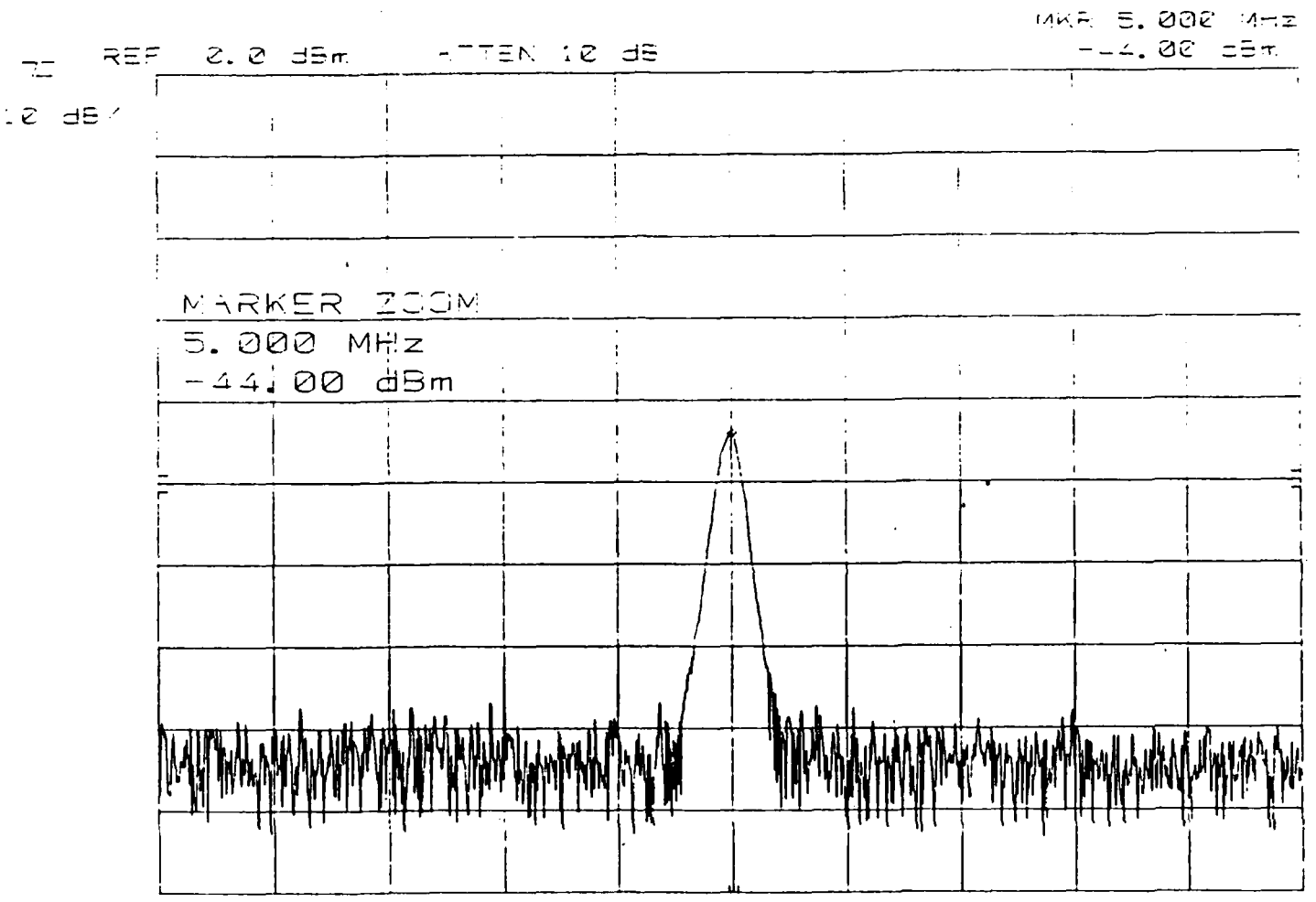


Figure 4.25 5 MHz Signal After 1511 Meters

This set of data also showed that on the average, depending on the orientation of the fiber, a connector loss of 1.25 db could be anticipated for a professionally manufactured cable. This figure will be used in the calculation of ideal link distances.

F. LINK DISTANCES

One of the limiting features in using the RS232 link is that it is limited to a maximum length of 50 feet for baud rates in excess of 300 baud [Ref. 8:p. 169]. With the utilization of a fiber optic network lengths could be increased to nearly 100 times that, for any baud rate that the DTEs are capable of transmitting and receiving.

A link distance was calculated for 50/125 micrometer graded index fiber with a loss of 7 db/km. Using the manufacturer's specification the optical power coupled into the fiber would be -20.0 dbm. The maximum rated sensitivity for the detector, -25 dbm as specified by the manufacturer [Ref. 7:p.13]. An average connector loss of 1.25 db per connector was measured and was used in the calculations. An optical budget of 7.0 db was obtained through these calculations, (transmitted power - (connector loss + receiver sensitivity)). This would provide a link distance of 1.00 kilometer.

Experimentally, using 200 meters of 50/125 micrometer graded index fiber, at 7db/km loss, and an attenuator (since greater lengths of 50/125 micrometer fiber were not available)

a link distance of 1.27 kilometers was obtained, an increase of 27.0% over design specifications.

For a 100/140 micrometer graded index fiber, at 7 db/km loss, the manufacturer's maximum designed optical transmitted power coupled into the fiber is -11.2 dbm. Using the specifications above, a calculated link of distance of 2.34 kilometers is possible.

Experimentally a link of distance 1.511 kilometers was achieved. A greater distance may have been achieved but the laboratory attenuator available was not suitable for use on the 100/140 micrometer fiber.

G. PRODUCT COMPARISON

A comparison of the costs and other major characteristics of this unit and other equivalent units is shown in Table VI. From analysis of Table VI it can be seen that the fiber optic unit described in this project is comparable to commercial units on the market in both price and in performance.

TABLE VI

PRODUCT COMPARISON

UNIT	MAX. FREQ.	MANNER OF OPERATION	TOTAL PRICE	LINK DIST.	EXPANDABILITY
FOM	5MHz	BI-DIRECTIONAL FULL DUPLEX	593.00	1.27 KM	YES (AT A COST OF 300.00 PER STATION)
HPIB	4.8MHz	HALF DUPLEX	2770.00	1.25 KM	YES (AT A COST OF 860.00 PER STATION)
ATT	19.2 KHz	BI-DIRECTIONAL FULL DUPLEX	520.00	1 KM	NO
LIT.	2 MHz	BI-DIRECTIONAL FULL DUPLEX	1998.00	8 KM	UNKNOWN

LEGEND:

FOM - FIBER OPTIC MODULES

HPIB - HEWLETT-PACKARD INTERFACE BUS EXTENDER [Ref. 14]

ATT - ATT ODL RS232-2 FIBER OPTIC MODEM [Ref. 15]

LIT. - LITTON INDUSTRY EO3671 [Ref. 16]

V. CONCLUSIONS

As can be seen from Table VI the link designed here would have capability of expanding because of the great bandwidth offered by the use of fibers.

The link presented in this thesis is a point to point link, but the same principles would apply to higher order networks. Stations could be added on this link, but it would be at a minimum cost of three hundred dollars per station. Another limitation of expanding onto a higher level network would be the optical power. The optical budget of each station would have to be observed to ensure that one station did not drain the optical bus of such a large amount of power to render the other taps useless.

Some possible solutions to this problem could be to interchange the LEDs in the CAFs with laser sources or to use more sensitive detectors. A different approach would to have each station at a differing wavelength within the CAF. The only problem with scheme would be that it would not be interactive.

In essence, this thesis is the beginning point of a possible inexpensive fiber optic local area network.

APPENDIX A

MOTOROLA MC1489 QUAD LINE RECEIVER DATA SHEETS

MOTOROLA

MC1489
MC1489A

QUAD LINE RECEIVERS

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

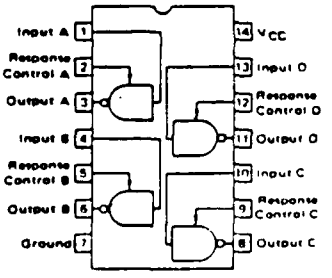
- Input Resistance – 3.0 k to 7.0 kilohms
- Input Signal Range – ± 30 Volts
- Input Threshold Hysteresis Built In
- Response Control
  a) Logic Threshold Shifting
  b) Input Noise Filtering

QUAD MDTL
LINE RECEIVERS
RS-232C

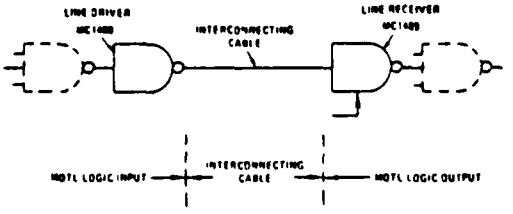
SILICON MONOLITHIC
INTEGRATED CIRCUIT

L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA

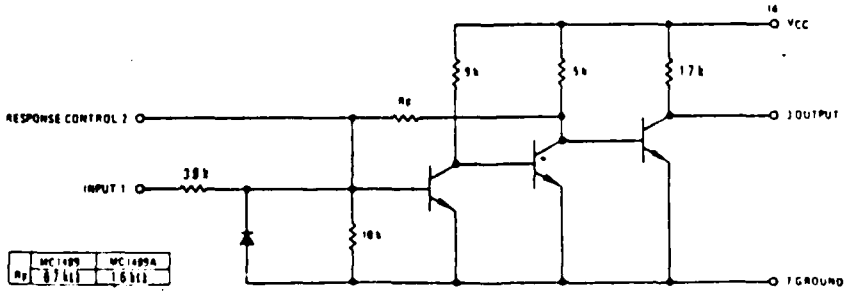
P SUFFIX
PLASTIC PACKAGE
CASE 646-05



TYPICAL APPLICATION



EQUIVALENT CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Input Voltage Range	V_{IR}	±30	Vdc
Output Load Current	I_L	20	mA
Power Dissipation (Package Limitation, Ceramic and Plastic Dual In-Line Package) Derate above T_A = +25°C	P_D $1/\theta JA$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (Response control pin is open.) (V_{CC} = +5.0 Vdc ± 10%, T_A = 0 to +75°C unless otherwise noted)

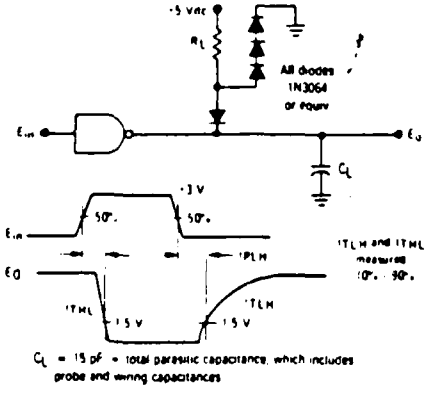
Characteristics		Symbol	Min	Typ	Max	Unit
Positive Input Current	(V_{IH} = +25 Vdc) (V_{IH} = +3.0 Vdc)	I_{IH}	3.6 0.43	— —	8.3 —	mA
Negative Input Current	(V_{IL} = -25 Vdc) (V_{IL} = -3.0 Vdc)	I_{IL}	-3.6 -0.43	— —	-8.3 —	mA
Input Turn-On Threshold Voltage (T_A = +25°C, V_{OL} ≤ 0.45 V)	MC1489 MC1489A	V_{IH}	1.0 1.75	— 1.95	1.5 2.25	Vdc
Input Turn-Off Threshold Voltage (T_A = +25°C, V_{OH} ≥ 2.5 V, I_L = -0.5 mA)	MC1489 MC1489A	V_{IL}	0.75 0.75	— 0.8	1.25 1.25	Vdc
Output Voltage High	(V_{IH} = 0.75 V, I_L = -0.5 mA) (Input Open Circuit, I_L = -0.5 mA)	V_{OH}	2.5 2.5	4.0 4.0	5.0 5.0	Vdc
Output Voltage Low	(V_{IL} = 3.0 V, I_L = 10 mA)	V_{OL}	—	0.2	0.45	Vdc
Output Short-Circuit Current		I_{OS}	—	-3.0	-4.0	mA
Power Supply Current (All Gates "on," I_{out} = 0 mA, V_{IH} = +5.0 Vdc)		I_{CC}	—	16	28	mA
Power Consumption	(V_{IH} = +5.0 Vdc)	P_C	—	80	130	mW

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 1%, T_A = +25°C, See Figure 1.)

Propagation Delay Time	(R_L = 3.9 kΩ)	t_{PLH}	—	25	85	ns
Rise Time	(R_L = 3.9 kΩ)	t_{TLH}	—	120	175	ns
Propagation Delay Time	(R_L = 390 Ω)	t_{PHL}	—	25	50	ns
Fall Time	(R_L = 390 Ω)	t_{THL}	—	10	20	ns

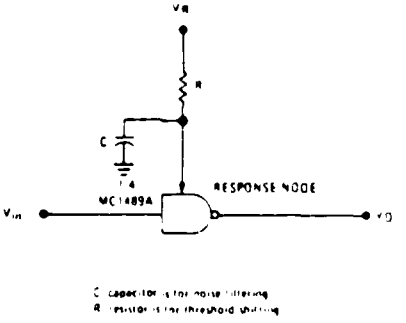
TEST CIRCUITS

FIGURE 1 — SWITCHING RESPONSE



C_L = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances

FIGURE 2 — RESPONSE CONTROL NODE



C = capacitor(s) for noise filtering
R = resistor(s) for threshold shifting

TYPICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 3 — INPUT CURRENT

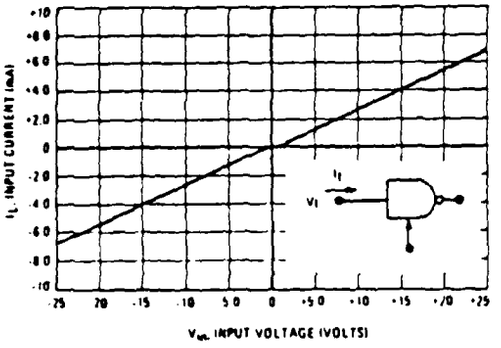


FIGURE 4 — MC1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT

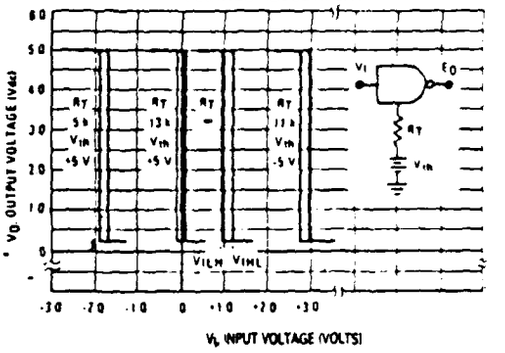


FIGURE 5 — MC1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT

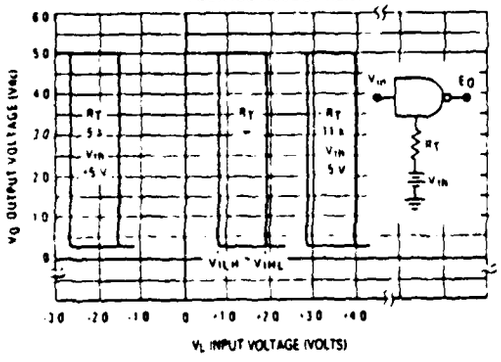


FIGURE 6 — INPUT THRESHOLD VOLTAGE versus TEMPERATURE

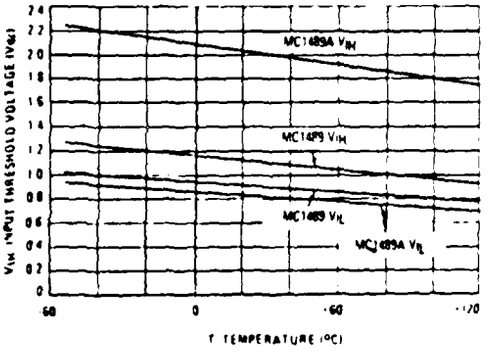
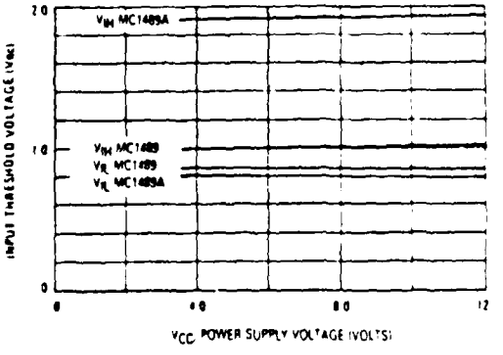


FIGURE 7 — INPUT THRESHOLD versus POWER-SUPPLY VOLTAGE



APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE}.

The receiver shall detect a voltage between −3.0 and −25 volts as a Logic "1" and inputs between +3.0 and +25 volts as a Logic "0." On some interchange leads, an open circuit of power "OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or Logic "1." For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25 volts and turn-off of 1.0 volt for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 volts and turn-off of 0.8 volt for typically 1.15 volts of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power-supply. Figures 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high-energy noise pulses. Figures 8 and 9 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 10)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

FIGURE 8 — TYPICAL TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

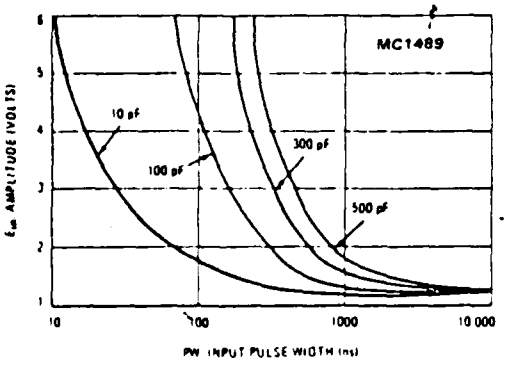
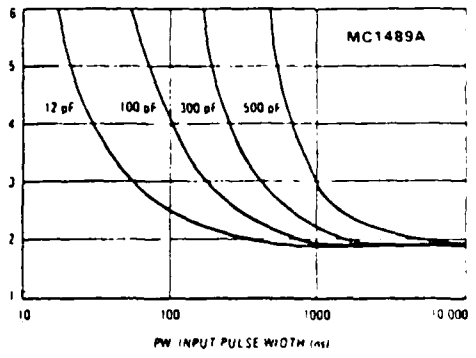


FIGURE 9 — TYPICAL TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND



APPLICATIONS INFORMATION (continued)

FIGURE 10 — TYPICAL TRANSLATOR APPLICATION — MOS TO DTL OR TTL

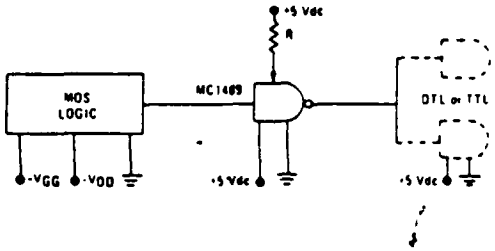
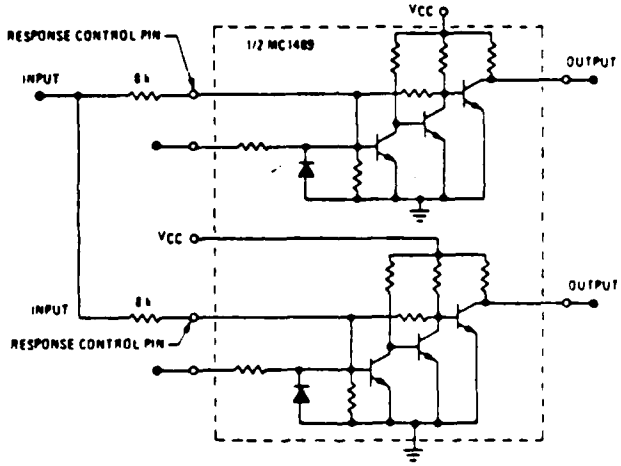


FIGURE 11 — TYPICAL PARALLELING OF TWO MC1489,A RECEIVERS TO MEET RS-232C



APPENDIX B

RCA LINEAR INTEGRATED CIRCUIT CA3127E HIGH FREQUENCY N-P-N TRANSISTOR ARRAY DATA SHEETS

CA3127E

High-Frequency N-P-N Transistor Array

For Low-Power Applications at Frequencies up to 500 MHz

RCA CA3127E* consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low 1/f noise and a value of f_T in excess of 1 GHz, making the CA3127E useful from dc to 500 MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127E provides close electrical and thermal matching of the five transistors.

The CA3127E is supplied in a 16-lead dual-in-line plastic package and operates over the full military temperature range of −55 to +125°C.

* Formerly RCA Dev. No. TA6206.

Features:

- Gain-Bandwidth Product (f_T) > 1 GHz
- Power Gain = 30 dB (typ.) at 100 MHz
- Noise Figure = 3.5 dB (typ.) at 100 MHz
- Five independent transistors on a common substrate

Applications:

- VHF amplifiers
- Multifunction combinations—RF/mixer/oscillator
- Sense amplifiers
- Synchronous detectors
- VHF mixers
- IF Converter
- IF amplifiers
- Synthesizers
- Cascade amplifiers

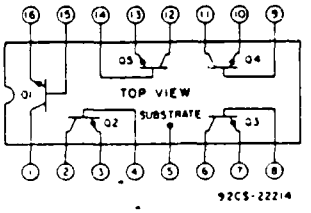


Fig. 1 – Schematic diagram of CA3127E.

MAXIMUM RATINGS,
Absolute-Maximum Values:

POWER DISSIPATION, P_D:
- Any one transistor . . . . . 85 mW
- Total Package:
- For T_A up to 75°C . . . . . 425 mW
- For T_A > 75°C Derate Linearly at . . . . . 6.67 mW/°C

AMBIENT TEMPERATURE RANGE
- Operating . . . . . −55 to +125°C
- Storage . . . . . −65 to +125°C

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . +265°C

The following ratings apply for each transistor in the device:
- Collector-to-Emitter Voltage, V_{CEO} . . . 15 V
- Collector-to-Base Voltage, V_{CBO} . . . 20 V
- Collector-to-Substrate Voltage, V_{CIO}* . . . 20 V
- Collector Current, I_C . . . 20 mA

*The collector of each transistor of the CA3127E is isolated from the substrate by an integral diode. The substrate (terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

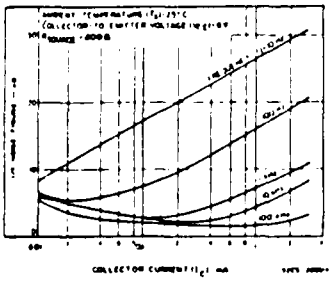


Fig. 2 – 1/f noise figure as a function of collector current at R_{SOURCE} = 500 Ω

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	TEST CONDITIONS		LIMITS Min.	Typ.	Max.	UNITS
For Each Transistor:						
Collector-to-Base Breakdown Voltage	I_C = 10 μA, I_E = 0		20	32	–	V
Collector-to-Emitter Breakdown Voltage	I_C = 1 mA, I_B = 0		15	24	–	V
Collector-to-Substrate Breakdown Voltage	I_{C1} = 10 μA, I_B = 0, I_E = 0		20	60	–	V
Emitter-to-Base Breakdown Voltage*	I_E = 10 μA, I_C = 0		4	5.7	–	V
Collector-Cutoff-Current	V_{CE} = 10 V, I_B = 0		–	–	0.5	μA
Collector-Cutoff-Current	V_{CB} = 10 V, I_E = 0		–	–	40	nA
DC Forward-Current Transfer Ratio	V_{CE} = 6 V	I_C = 5 mA	35	88	–	
		I_C = 1 mA	40	90	–	
		I_C = 0.1 mA	35	85	–	
Base-to-Emitter Voltage	V_{CE} = 6 V	I_C = 5 mA	0.71	0.81	0.91	V
		I_C = 1 mA	0.66	0.76	0.86	
		I_C = 0.1 mA	0.60	0.70	0.80	
Collector-to-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1 mA		–	0.26	0.50	V
Magnitude of Difference in V_{BE}	Q_1 & Q_2 Matched		–	0.5	5	mV
Magnitude of Difference in I_B	V_{CE} = 6 V, I_C = 1 mA		–	0.2	3	μA

*When used as a zener for reference voltage, the device must not be subjected to more than 0.1 millijoule of energy from any possible capacitance or electrostatic discharge in order to prevent degradation of the junction. Maximum operating zener current should be less than 10 mA.

DYNAMIC CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTICS	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
I/F Noise Figure	f = 100 kHz, R_S = 500 Ω, I_C = 1 mA	–	1.8	–	dB
Gain-Bandwidth Product	V_{CE} = 6 V, I_C = 5 mA	–	1.15	–	GHz
Collector-to-Base Capacitance	V_{CB} = 6 V, f = 1 MHz	–	See	–	pF
Collector-to-Substrate Capacitance	V_{CI} = 6 V, f = 1 MHz	–	Fig.	–	pF
Emitter-to-Base Capacitance	V_{BE} = 4 V, f = 1 MHz	–	5	–	pF
Voltage Gain	V_{CE} = 6 V, f = 10 MHz, R_L = 1 kΩ, I_C = 1 mA	–	28	–	dB
Power Gain	Cascode Configuration f = 100 MHz, V^+ = 12 V	27	30	–	dB
Noise Figure	I_C = 1 mA	–	3.5	–	dB
Input Resistance	Common-Emitter	–	400	–	Ω
Output Resistance	Configuration	–	4.6	–	kΩ
Input Capacitance	V_{CE} = 6 V	–	3.7	–	pF
Output Capacitance	I_C = 1 mA	–	2	–	pF
Magnitude of Forward Transadmittance	f = 200 MHz	–	24	–	mmho

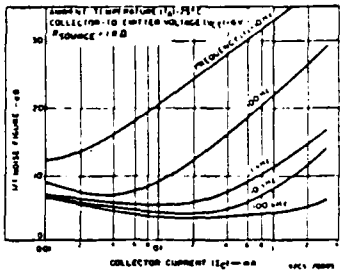


Fig. 3 – 1/f noise figure as a function of collector current at R_{SOURCE} = 1 kΩ.

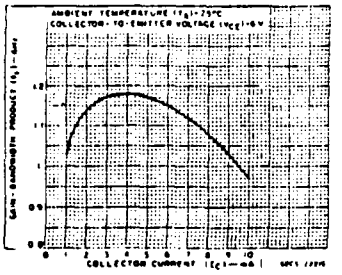


Fig. 4 – Gain-bandwidth product as a function of collector current.

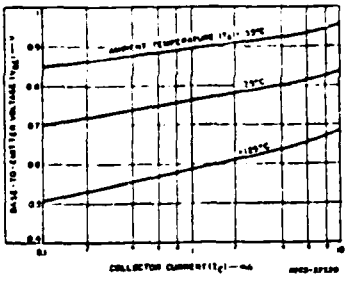


Fig. 5 – Base-to-emitter voltage as a function of collector current.

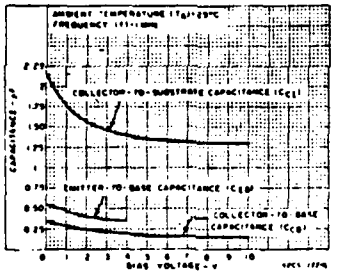


Fig. 6(a) – Capacitance as a function of bias voltage for Q_2.

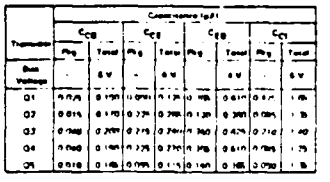


Fig. 6(b) – Typical capacitance values at f = 1 MHz. Three terminal measurement. Guard all terminals except those under test.

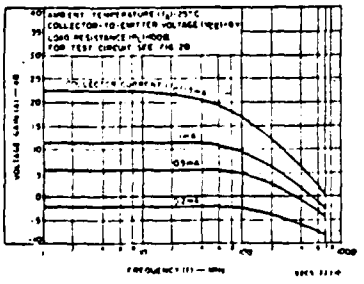


Fig. 7 – Voltage gain as a function of frequency at R_L = 100 Ω.

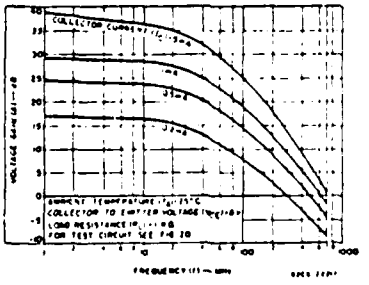


Fig. 8 – Voltage gain as a function of frequency at R_L = 1 kΩ.

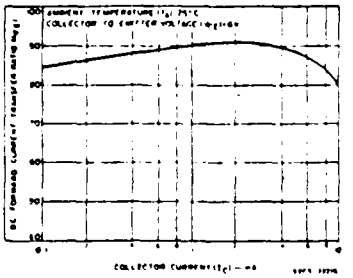


Fig. 9 – DC forward current transfer ratio as a function of collector current.

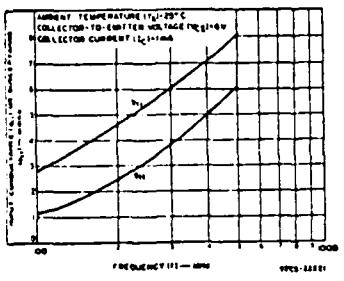


Fig. 10 – Input admittance (Y_{11}) as a function of frequency.

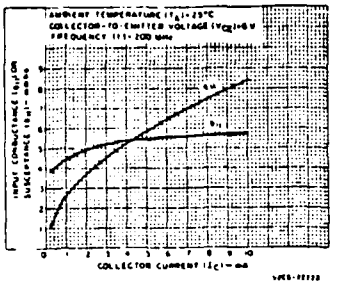


Fig. 11 – Input admittance (Y_{11}) as a function of collector current.

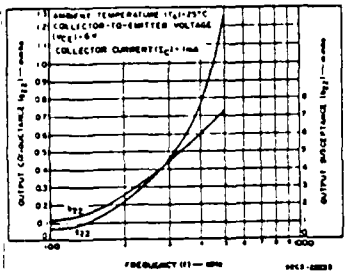


Fig. 12 – Output admittance (Y_{22}) as a function of frequency.

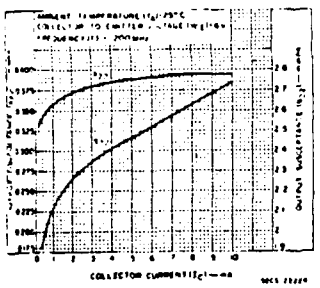


Fig. 13 – Output admittance (Y_{22}) as a function of collector current.

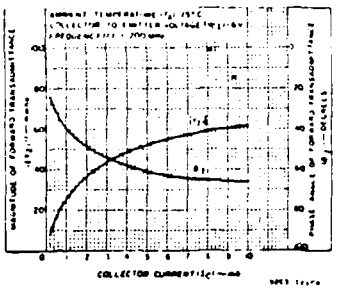


Fig. 14 – Forward transadmittance (Y_{21}) as a function of collector current.

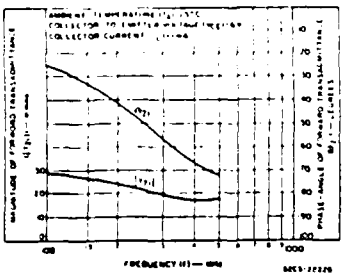


Fig. 15 – Forward transadmittance (Y_{21}) as a function of frequency.

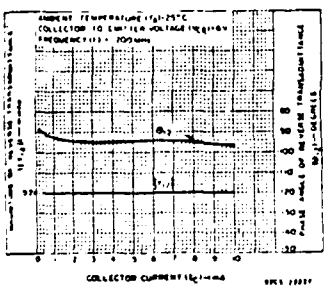


Fig. 16 – Reverse transadmittance (Y_{12}) as a function of collector current.

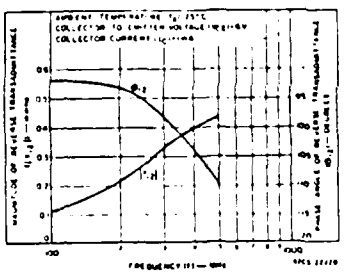


Fig. 17 – Reverse transadmittance (Y_{12}) as a function of frequency.

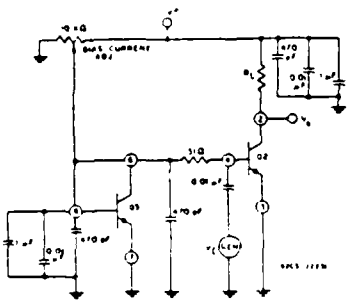


Fig. 18 – Voltage-gain test circuit using current-mirror biasing for Q_2.

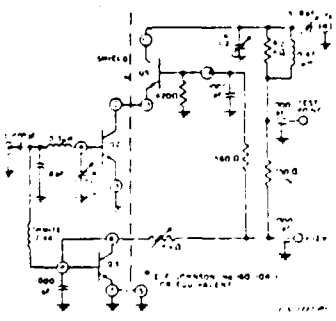


Fig. 19 – 100 MHz power gain and noise-figure test circuit.

This circuit was chosen because it conveniently represents a close approximation in performance to a properly unilateralized single transistor of this type. The use of Q3 in a current mirror configuration facilitates simplified biasing. The use of the cascode circuit in no way implies that the transistors cannot be used individually.

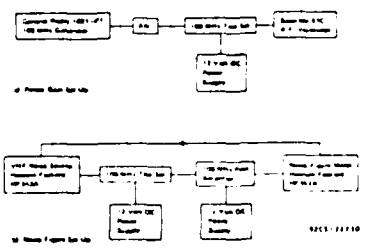


Fig. 20 – Block diagrams of power gain and noise-figure test set ups.

APPENDIX C

MOTOROLA MC1488 QUAD LINE DRIVER DATA SHEETS

MOTOROLA

MC1488

QUAD LINE DRIVER

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

Features:

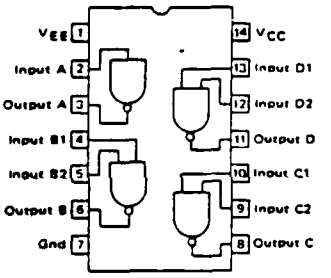
- Current Limited Output
  ±10 mA typ
- Power-Off Source Impedance
  300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All Motorola MDTL and MTTL Logic Families

QUAD MDTL LINE DRIVER
RS-232C
SILICON MONOLITHIC
INTEGRATED CIRCUIT

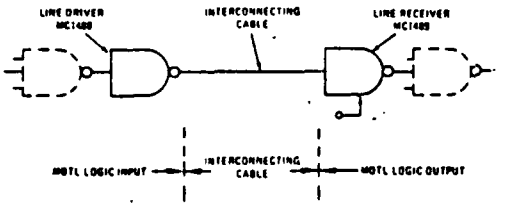
L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA

P SUFFIX
PLASTIC PACKAGE
CASE 646-05

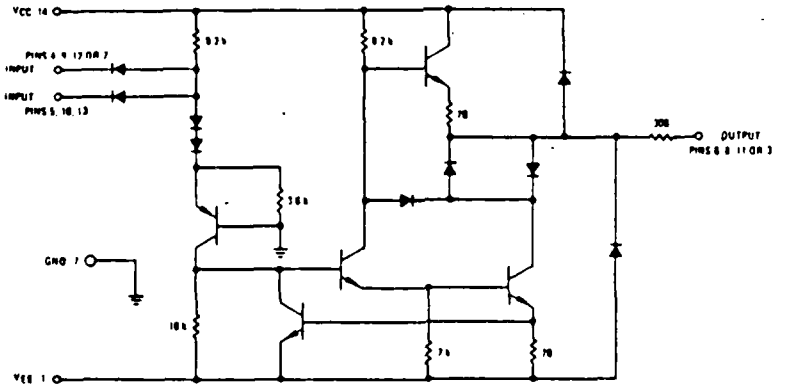
PIN CONNECTIONS



TYPICAL APPLICATION



CIRCUIT SCHEMATIC
(1/4 OF CIRCUIT SHOWN)



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+15 -15	Vdc
Input Voltage Range	V_{IR}	$-15 \leq V_{IR} \leq 7.0$	Vdc
Output Signal Voltage	V_O	±15	Vdc
Power Derating (Package Limitation, Ceramic and Plastic Dual-In-Line Package) Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +9.0 ±10% Vdc, V_{EE} = -9.0 ±10% Vdc, T_A = 0 to 75°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Current – Low Logic State (V_{IL} = 0)	1	I_{IL}		1.0	1.6	mA
Input Current – High Logic State (V_{IH} = 5.0 V)	1	I_{IH}			10	µA
Output Voltage – High Logic State	2	V_{OH}				Vdc
(V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = -9.0 Vdc)			+6.0	+7.0		
(V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = -13.2 Vdc)			+9.0	+10.5		
Output Voltage – Low Logic State	2	V_{OL}				Vdc
(V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = -9.0 Vdc)			-6.0	-7.0	-	
(V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = -13.2 Vdc)			-9.0	-10.5	-	
Positive Output Short Circuit Current (1)	3	I_{OS+}	+6.0	+10	+12	mA
Negative Output Short Circuit Current (1)	3	I_{OS-}	-6.0	-10	-12	mA
Output Resistance (V_{CC} = V_{EE} = 0, $\lvert V_O \rvert$ = +2.0 V)	4	r_o	300	-		Ohms
Positive Supply Current (R_L = ∞)	5	I_{CC}				mA
(V_{IH} = 1.9 Vdc, V_{CC} = +9.0 Vdc)			-	+15	+20	
(V_{IL} = 0.8 Vdc, V_{CC} = +9.0 Vdc)			-	+4.5	+6.0	
(V_{IH} = 1.9 Vdc, V_{CC} = +12 Vdc)			-	+19	+25	
(V_{IL} = 0.8 Vdc, V_{CC} = +12 Vdc)			-	+5.5	+7.0	
(V_{IH} = 1.9 Vdc, V_{CC} = +15 Vdc)			-	-	+34	
(V_{IL} = 0.8 Vdc, V_{CC} = +15 Vdc)			-	-	+12	
Negative Supply Current (R_L = ∞)	5	I_{EE}				
(V_{IH} = 1.9 Vdc, V_{EE} = -9.0 Vdc)			-	-13	-17	mA
(V_{IL} = 0.8 Vdc, V_{EE} = -9.0 Vdc)			-	-	-15	µA
(V_{IH} = 1.9 Vdc, V_{EE} = -12 Vdc)			-	-18	-23	mA
(V_{IL} = 0.8 Vdc, V_{EE} = -12 Vdc)			-	-	-15	µA
(V_{IH} = 1.9 Vdc, V_{EE} = -15 Vdc)			-	-	-34	mA
(V_{IL} = 0.8 Vdc, V_{EE} = -15 Vdc)			-	-	-25	mA
Power Consumption		P_C				mW
(V_{CC} = 9.0 Vdc, V_{EE} = -9.0 Vdc)			-	-	333	
(V_{CC} = 12 Vdc, V_{EE} = -12 Vdc)			-	-	576	

SWITCHING CHARACTERISTICS (V_{CC} = +9.0 ± 1% Vdc, V_{EE} = -9.0 ± 1% Vdc, T_A = +25°C.)

Propagation Delay Time (z_l = 3.0 k and 15 pF)	6	t_{PLH}	-	275	350	ns
Fall Time (z_l = 3.0 k and 15 pF)	6	t_{THL}	-	45	75	ns
Propagation Delay Time (z_l = 3.0 k and 15 pF)	6	t_{PHL}	-	110	175	ns
Rise Time (z_l = 3.0 k and 15 pF)	6	t_{TLH}	-	55	100	ns

(1) Maximum Package Power Dissipation may be exceeded if all outputs are shorted simultaneously.

CHARACTERISTIC DEFINITIONS

FIGURE 1 – INPUT CURRENT

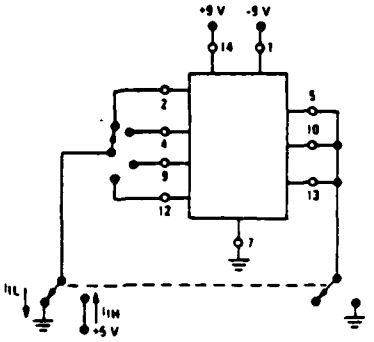


FIGURE 2 – OUTPUT VOLTAGE

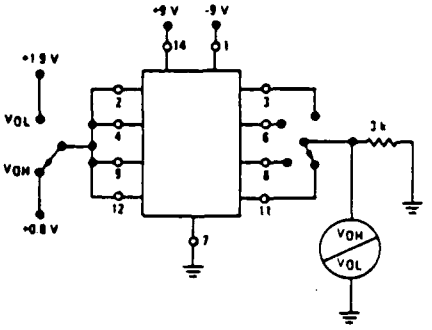


FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

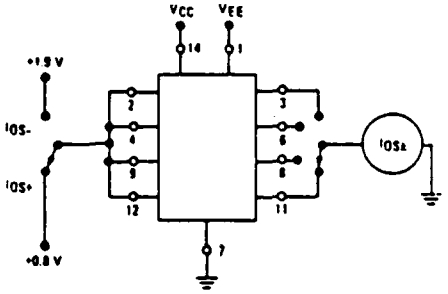


FIGURE 4 – OUTPUT RESISTANCE (POWER-OFF)

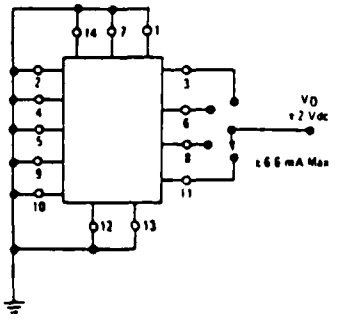


FIGURE 5 – POWER-SUPPLY CURRENTS

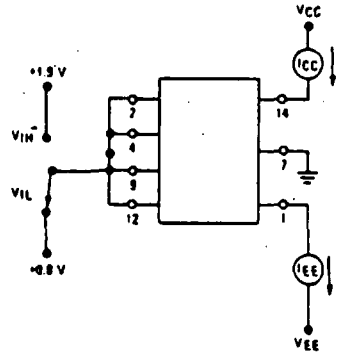
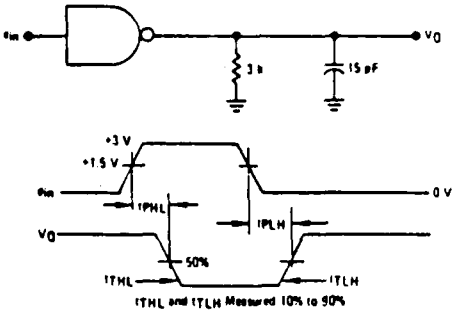


FIGURE 6 – SWITCHING RESPONSE



TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 7 – TRANSFER CHARACTERISTICS versus POWER-SUPPLY VOLTAGE

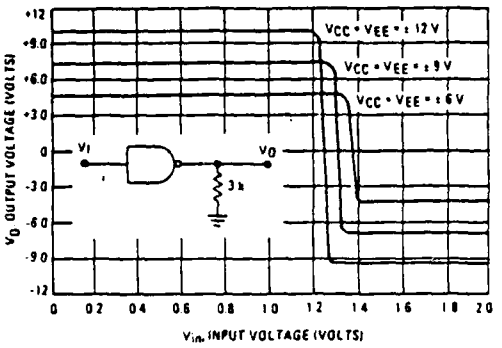


FIGURE 8 – SHORT-CIRCUIT OUTPUT CURRENT versus TEMPERATURE

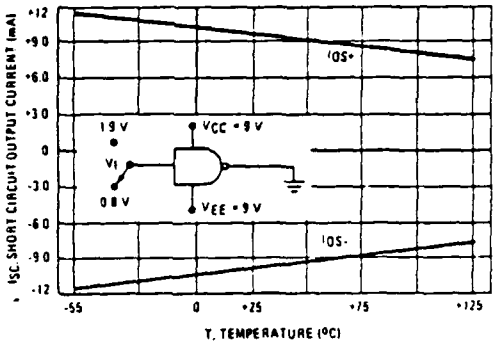


FIGURE 9 – OUTPUT SLEW RATE versus LOAD CAPACITANCE

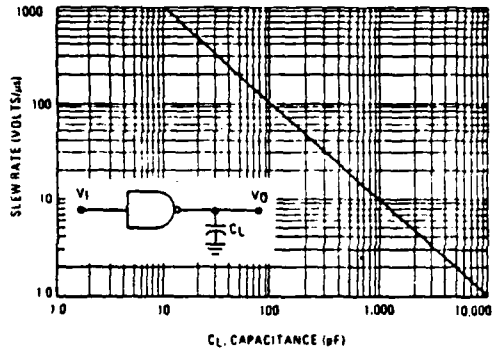


FIGURE 10 – OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS

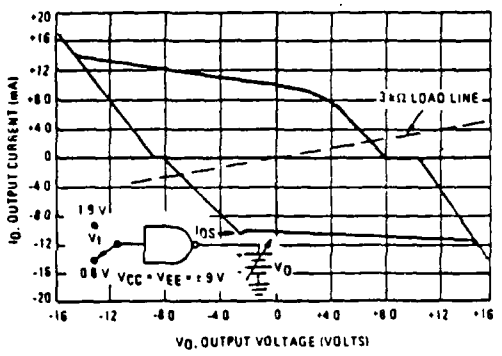
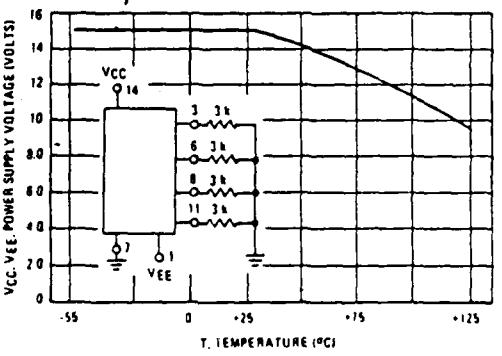


FIGURE 11 – MAXIMUM OPERATING TEMPERATURE versus POWER-SUPPLY VOLTAGE



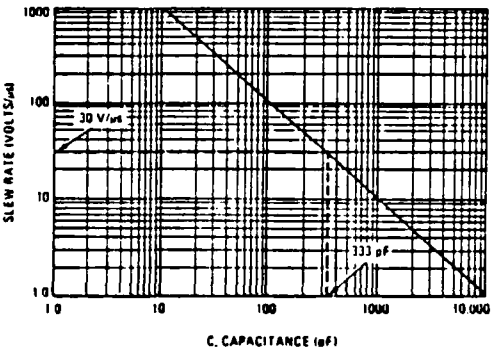
APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) RS232C specification detail the requirements for the interface between date processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15-volts in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 volts per microsecond. The inherent slew rate of the MC1488 is much too

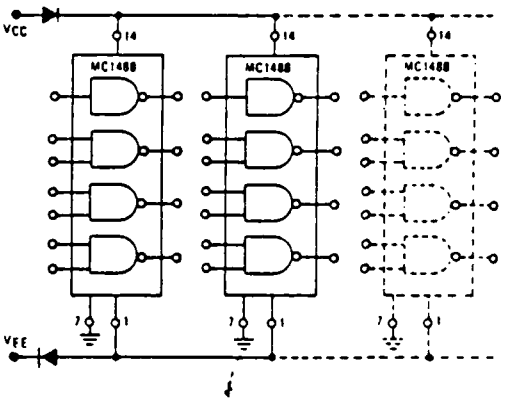
FIGURE 12 – SLEW RATE versus CAPACITANCE FOR I_{SC} = 10 mA



fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 12 is derived. Accordingly, a 330 pF capacitor on each output will guarantee a worst case slew rate of 30 volts per microsecond.

The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15-volt, 500-mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V_{CC} \geq 9.0$ V; $V_{EE} \leq -9.0$ V). In some power-supply designs, a loss of system power causes a low impedance on the power supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300-ohm output resistors to ground. If all four outputs were then shorted to plus or minus 15 volts, the power dissipation in these resistors

FIGURE 13 – POWER-SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS



would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±25-volt limits specified in the earlier Standard RS232B.) The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0 volts stated above.

The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Other Applications

The MC1488 is an *extremely versatile line driver* with a myriad of possible applications. Several features of the drivers enhance this versatility.

1. Output Current Limiting – this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488 used as a DTL to MOS translator where the high-level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.

2. Power Supply Range – as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately -2.5 volts to the minimum specified -15 volts. The MC1488 will drive the output to within 2 volts of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving RS232C lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 15 shows one such combination.

FIGURE 14 – MDTL/MTTL-TO-MOS TRANSLATOR

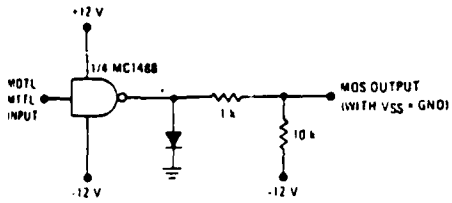
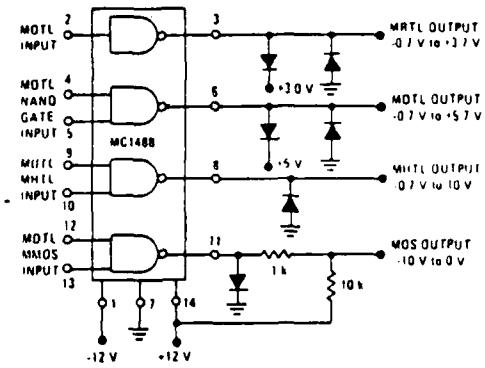


FIGURE 15 – LOGIC TRANSLATOR APPLICATIONS



LIST OF REFERENCES

1. Powers, J.P., AN INTRODUCTION TO FIBER OPTIC SYSTEMS Course Notes, Naval Postgraduate School, 1986.

2. Wolf, H.F. and others, HANDBOOK OF FIBER OPTICS : THEORY AND APPLICATIONS, p. 412, Garland STPM Press, 1979.

3. Roberts, H. and Rando, J., "WDM ACTIVE COUPLER FACILITATES BIDIRECTIONAL TRANSMISSION", LASER FOCUS, v.22, p. 100, APRIL 1986.

4. Stone, H.S., MICROCOMPUTER INTERFACING, Addison-Wesley Co., Inc., 1983.

5. Gofton, P.W., Mastering Serial Communications, SYBEX Inc., 1986.

6. Seyer, M.D., RS232 MADE EASY, Prentice-Hall Inc., 1984.

7. ADC FIBER OPTIC TRANSCEIVER EVALUATION KIT INSTRUCTION MANUAL, ADC Fiber Optics, 1986.

8. HP82939A Serial Interface Owner's Manual Series 80, Hewlett-Packard Co.,Inc., 1982.

9. SPINWRITER 7700 Terminals Product Description, NEC Information Systems Inc., 1981.

10. AMPEX 210 Video Display Terminal Operation Manual, AMPEX Corporation, Computer Products Division, 1984.

11. Motorola Linear Interface / Linear Devices, Motorola Inc., 1987.

12. Photodyne 22XLA Manual, p. iv, Photodyne Inc.

13. Connectorized Active Bi-directional Coupler Data Sheet, p. 2, ADC Fiber Optics, 1986.

14. Electronic Measurement Design Computation Catalog, p. 136, Hewlett-Packard Co., Inc., 1987.

15. ODL RS232 Fiber Optic Modem Preliminary Data Sheet, ATT, 1986.

16. Ormond, T., " Military Fiber Optic Components ", EDN,v.32, pp. 114-125, August 20 1987.

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